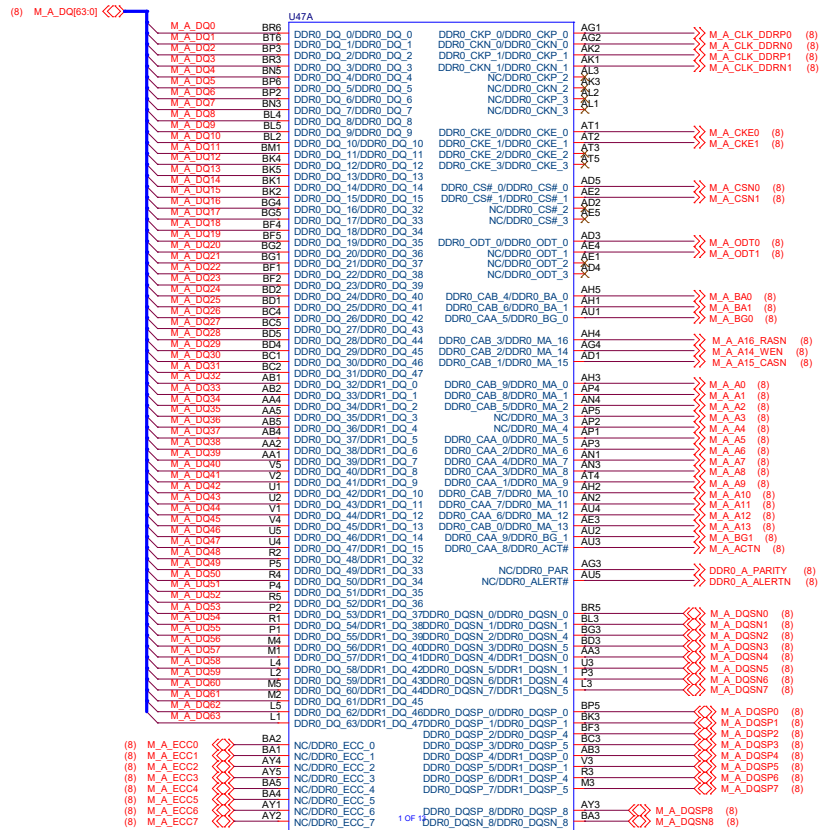
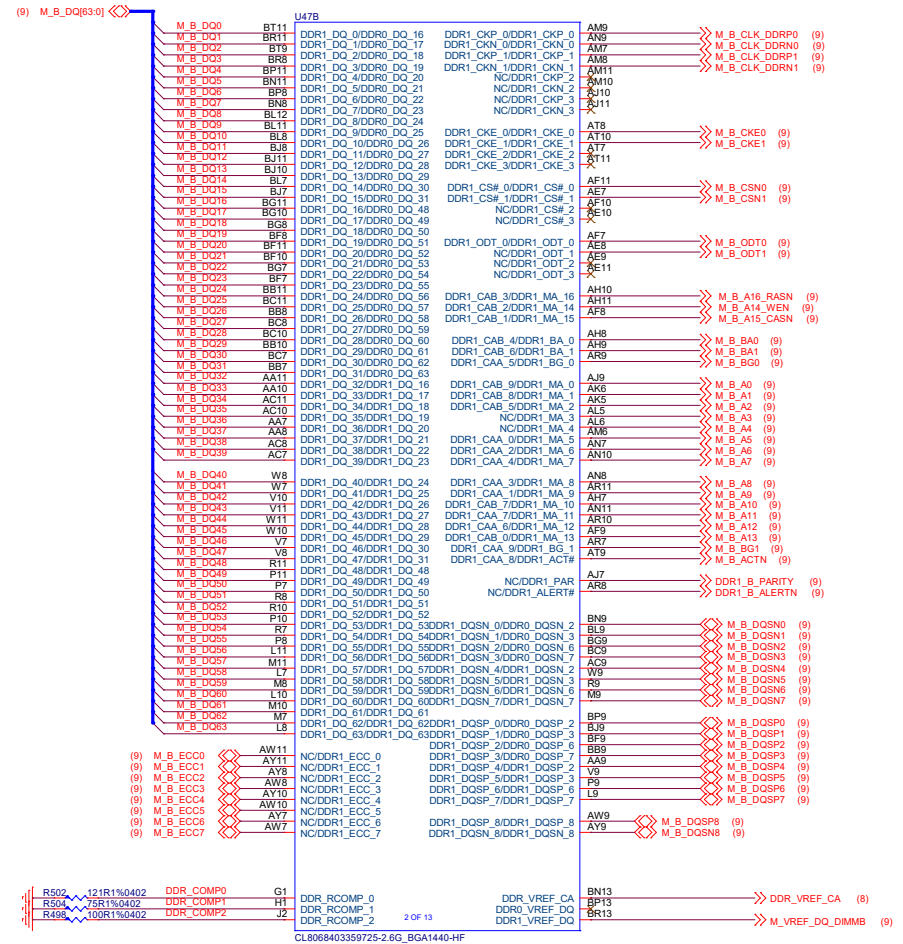
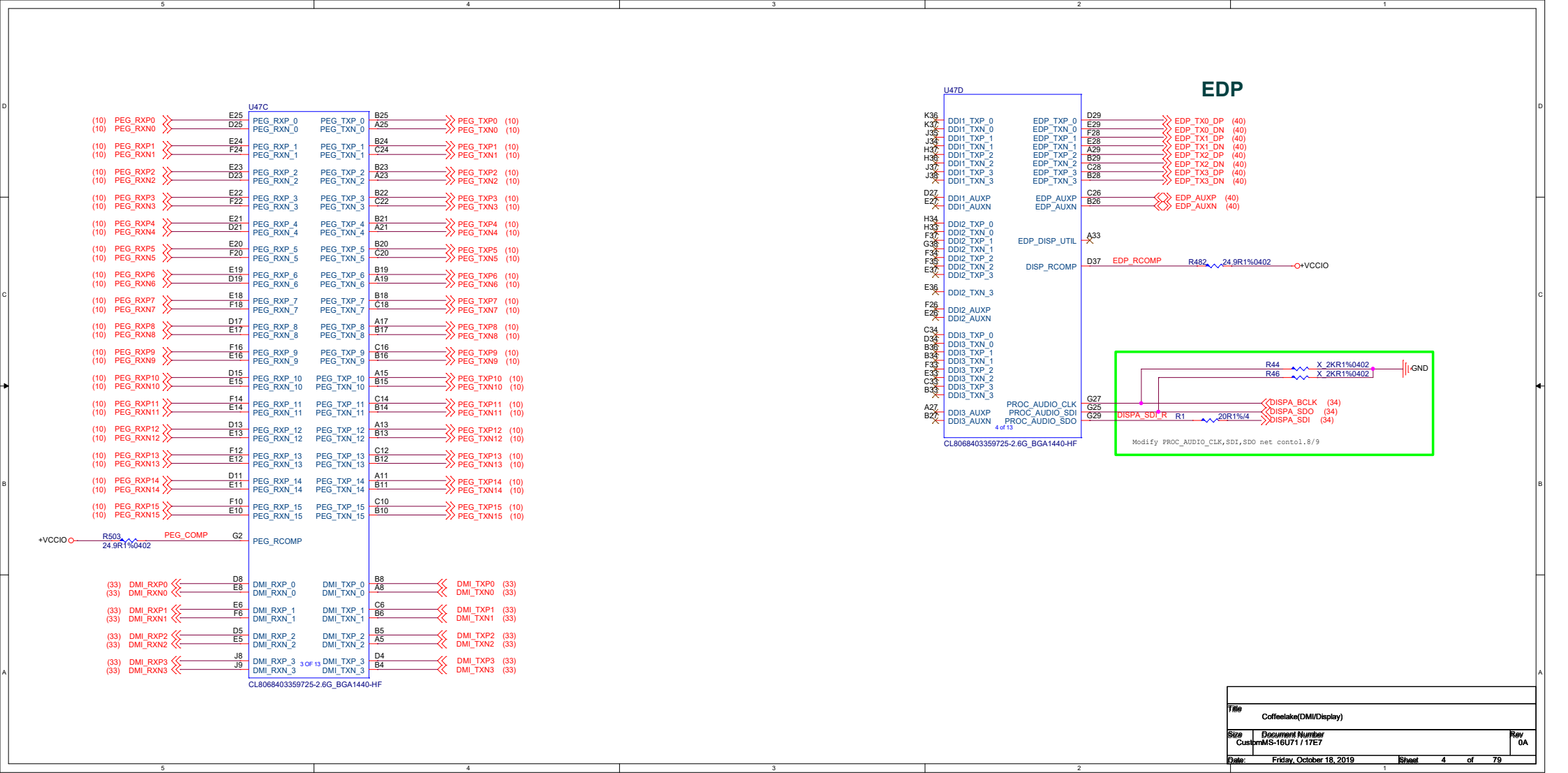


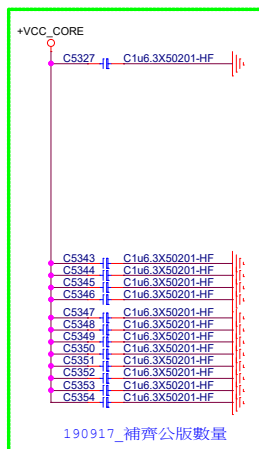
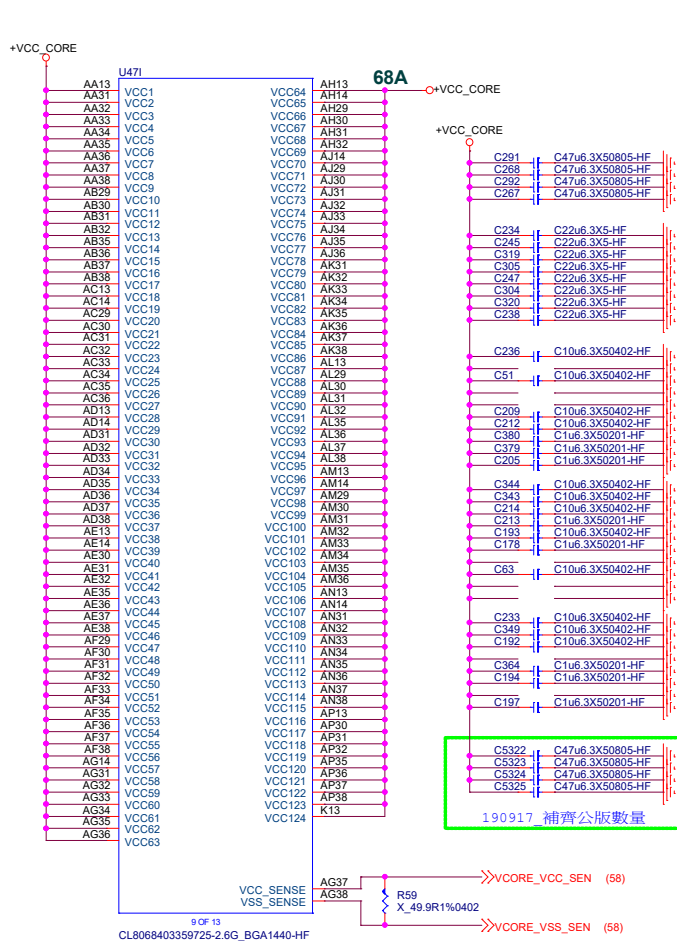
DDR Channel A



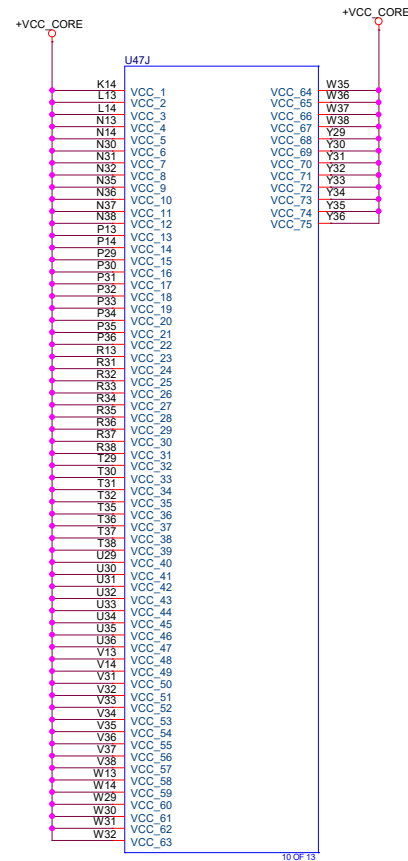
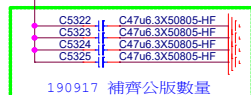
DDR Channel B



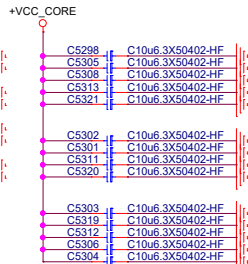
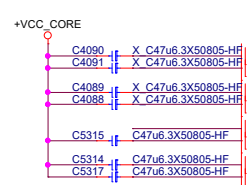
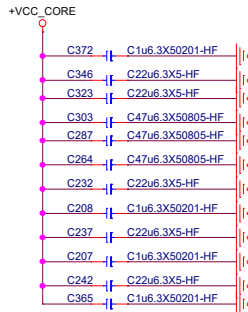
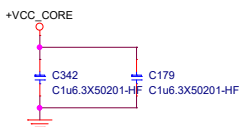
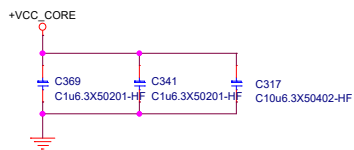
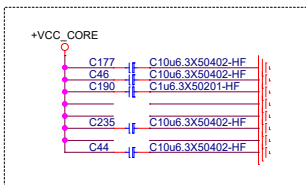


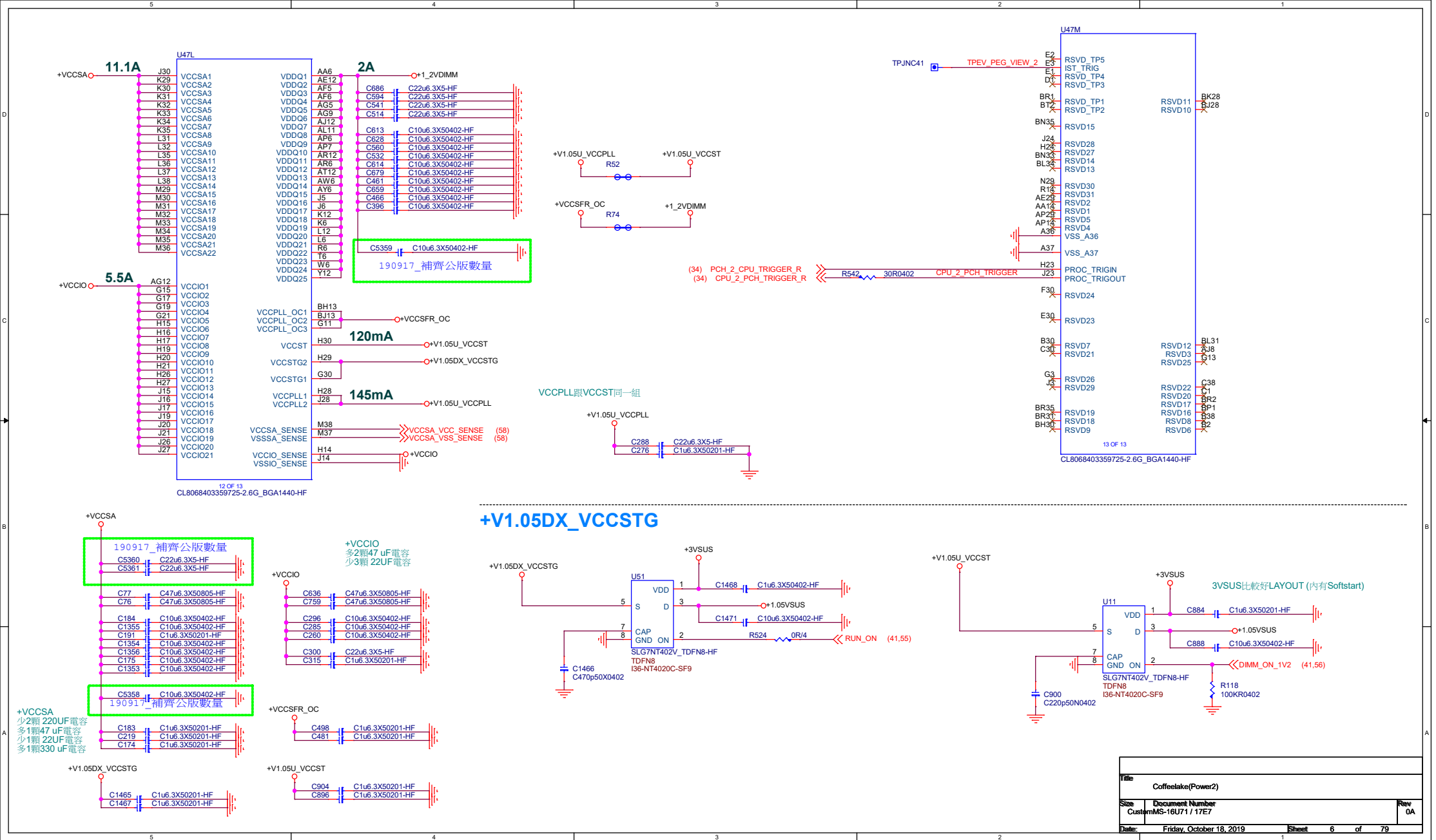


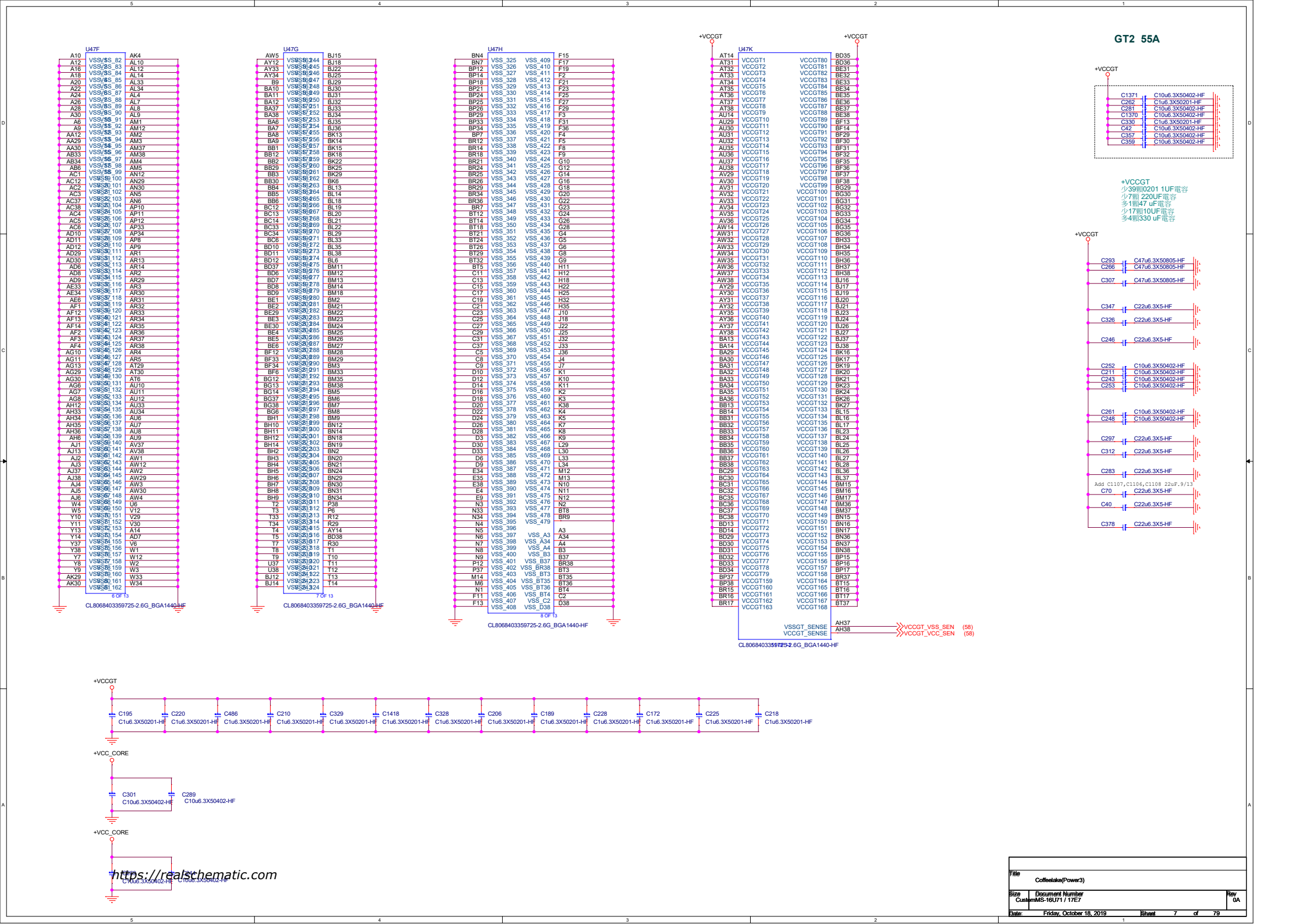
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少5顆 220uF電容
多8顆10 uF電容
多4顆330 uF電容



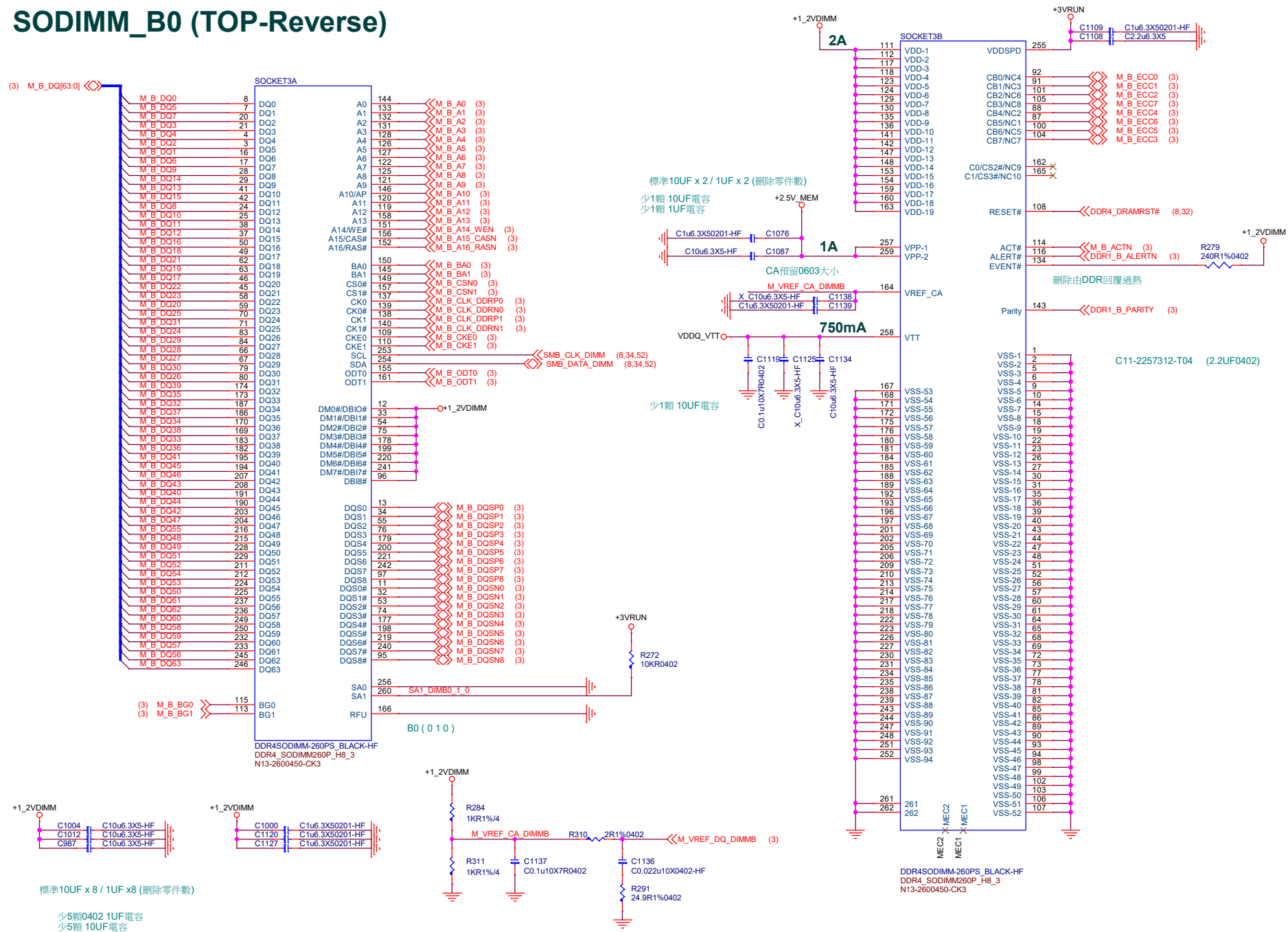
PATH MS-1541 ADD CAP



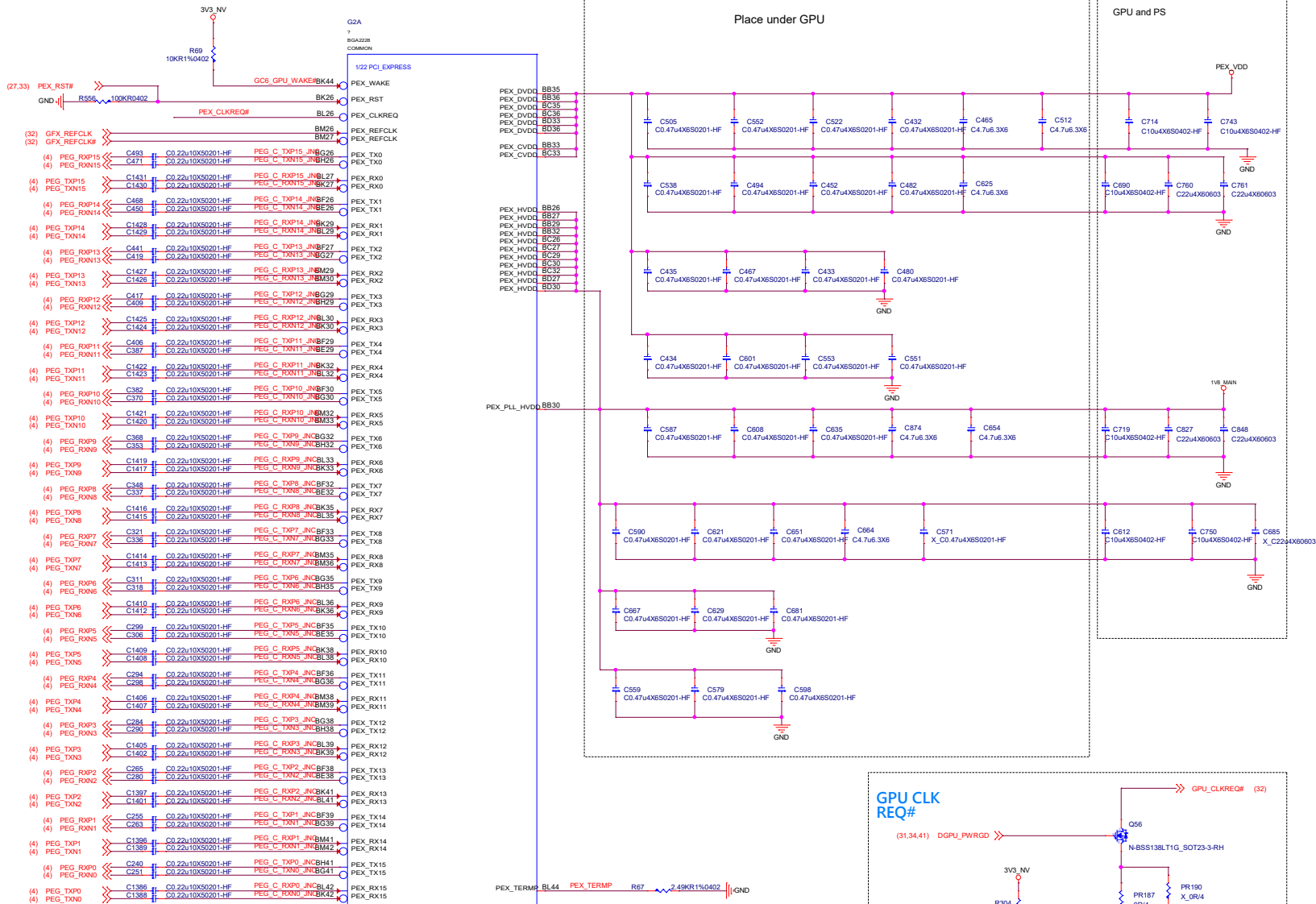


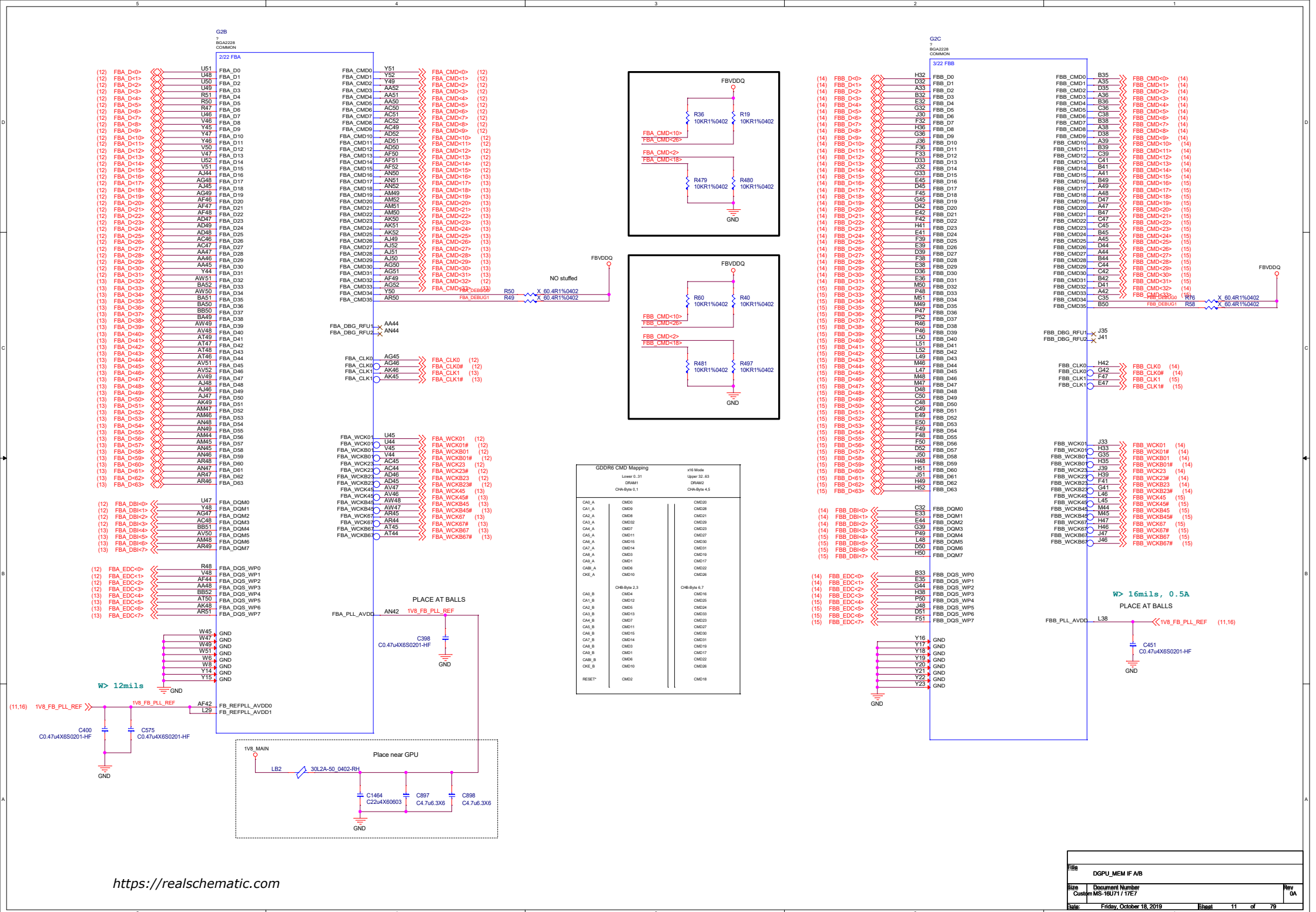


SODIMM_B0 (TOP-Reverse)

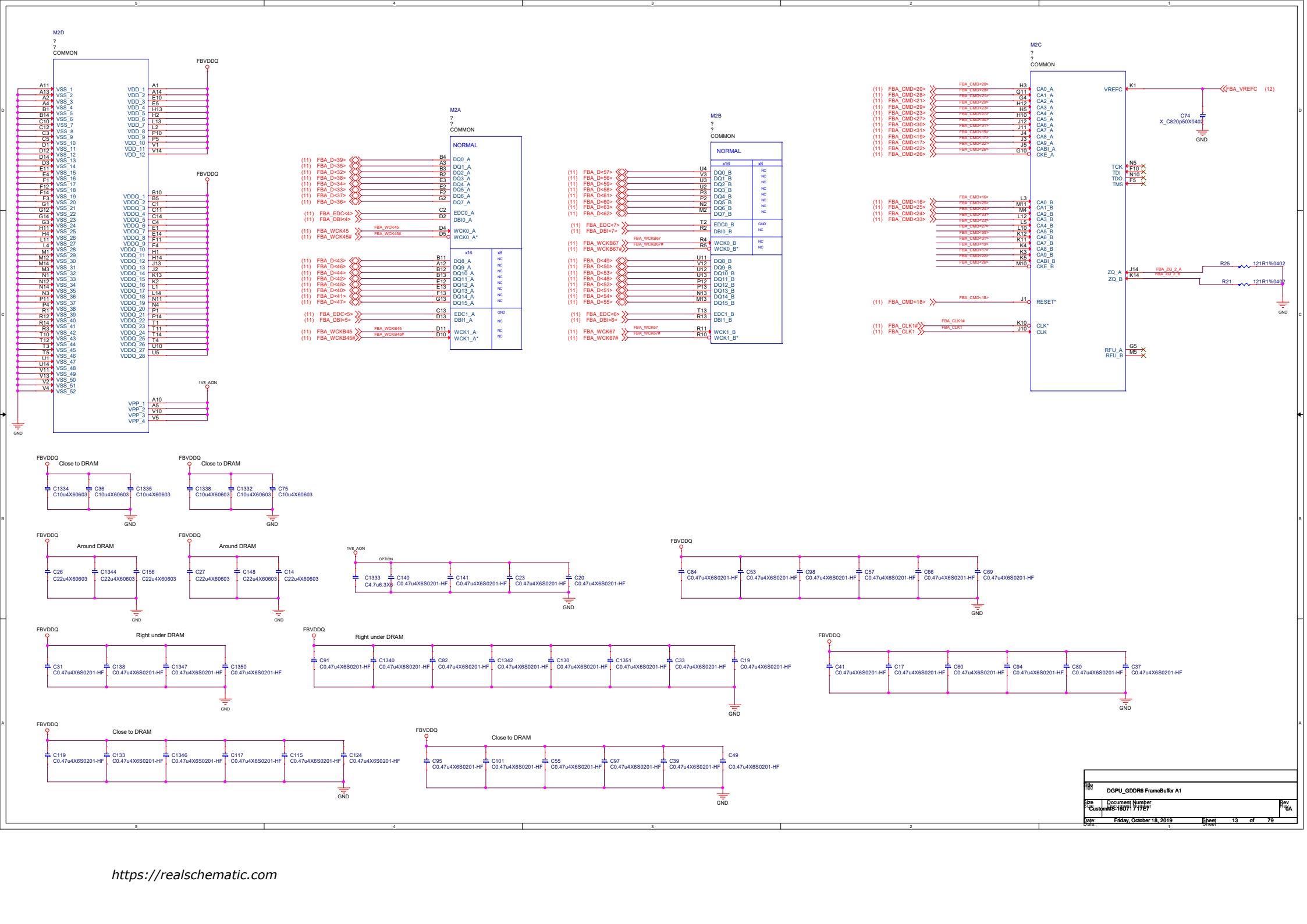


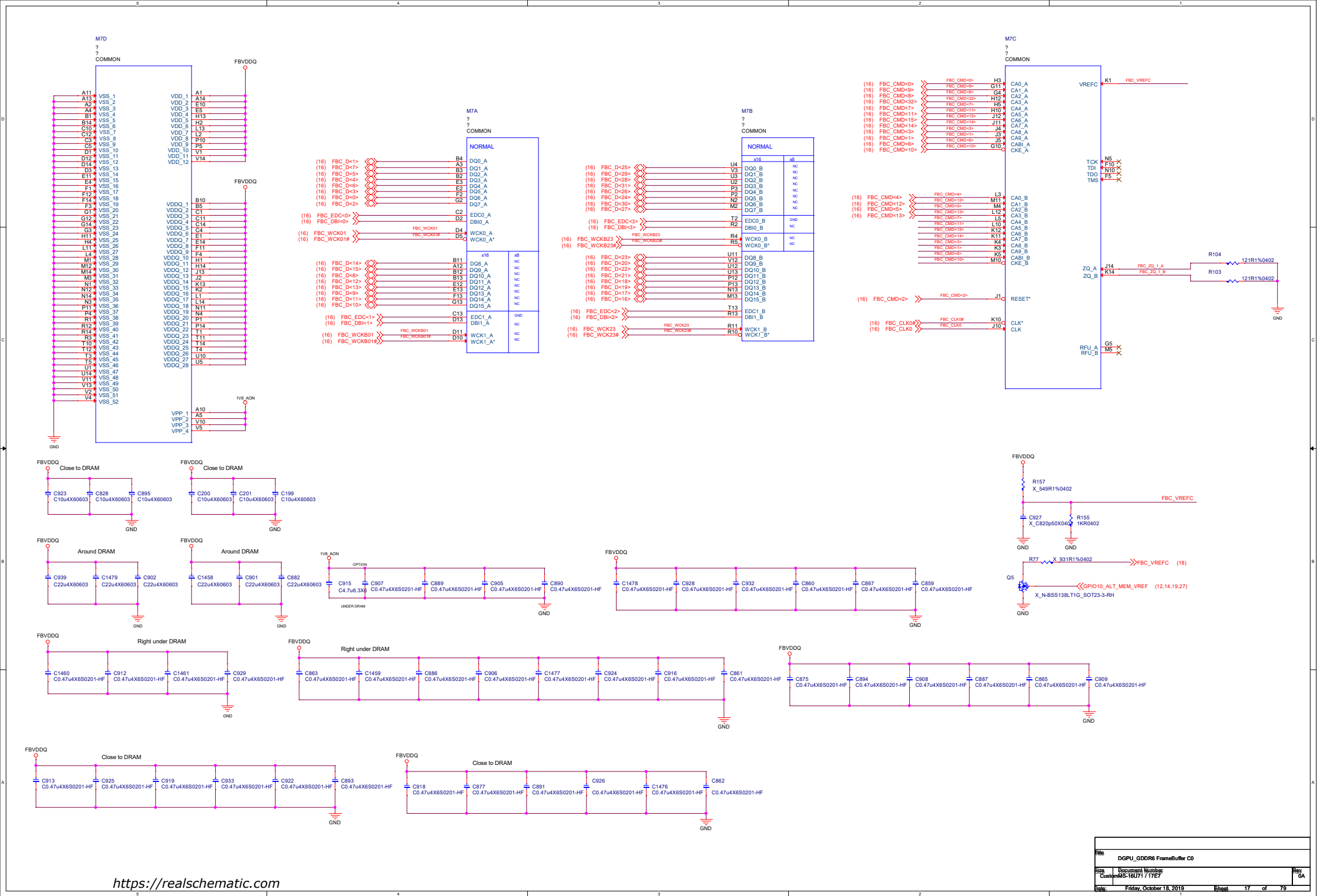
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DDR4_SODIMM_B0			
Size	Document Number		Rev
Custom	MS-16U71 / 17E7		0A
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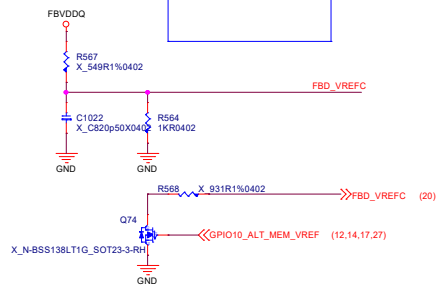
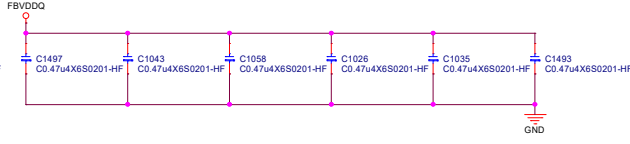
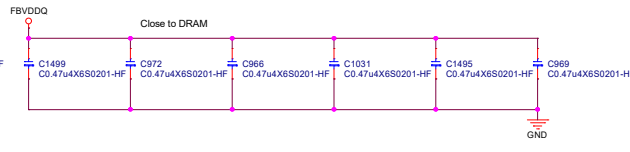
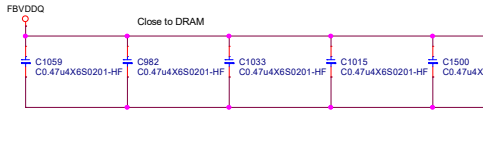
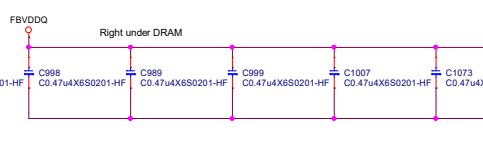
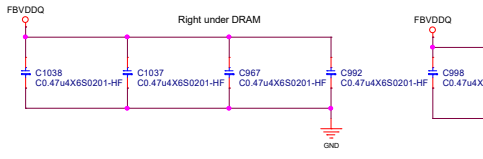
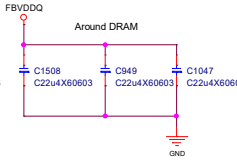
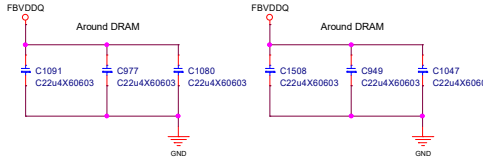
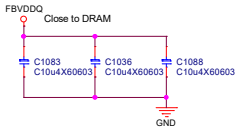
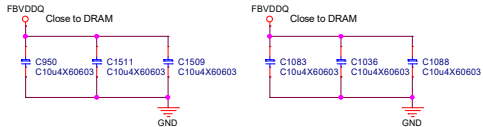
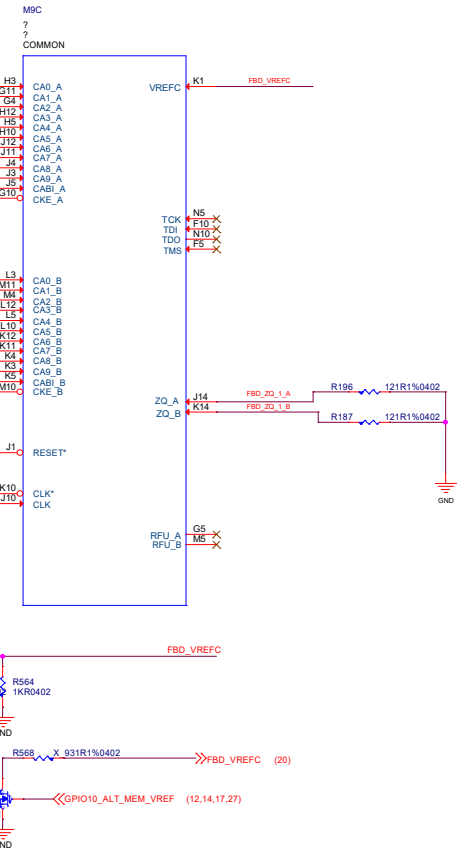
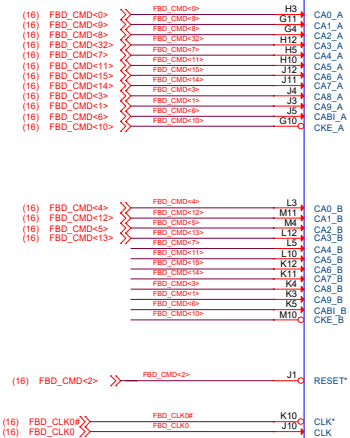
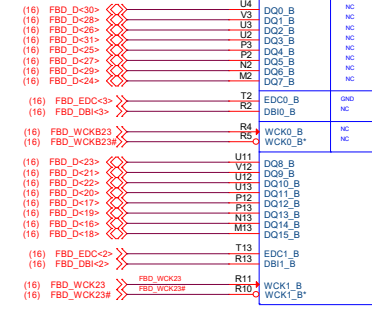
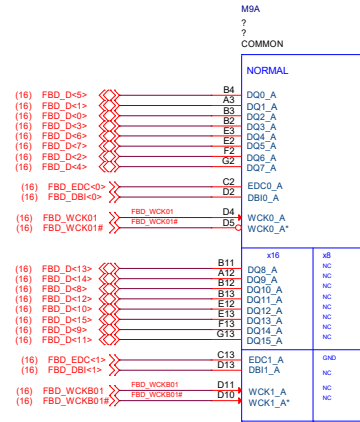
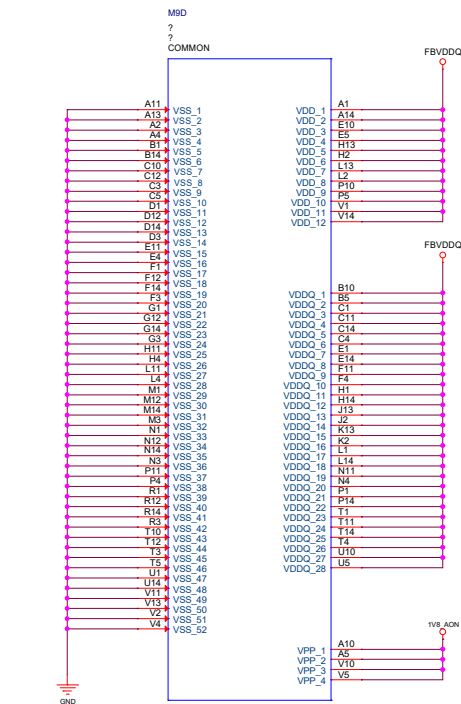












GPU PWR GND NCs

G2M
? BGA2228 COMMON

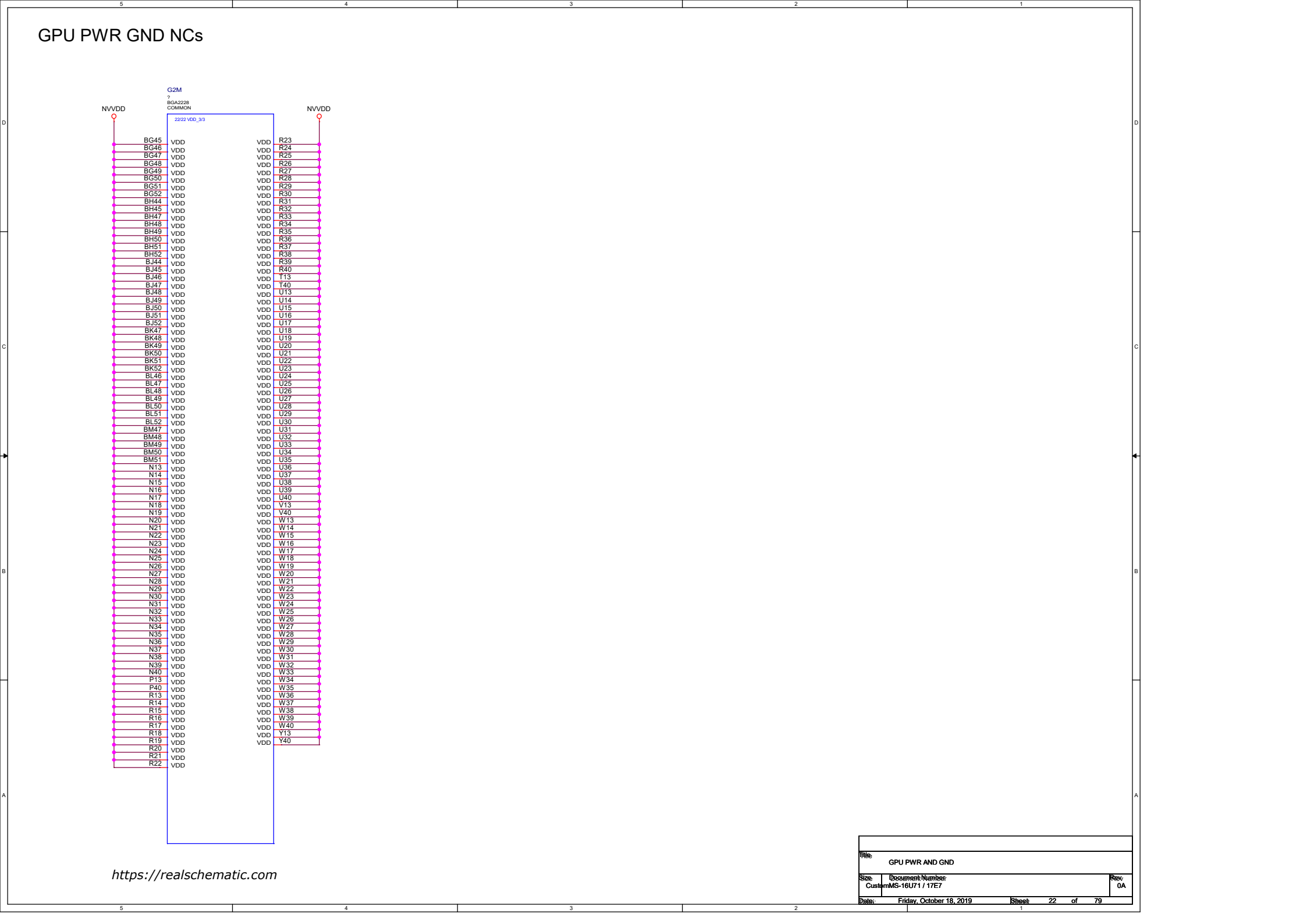
NVVD VDD NVVD

2222 VDD_3/3

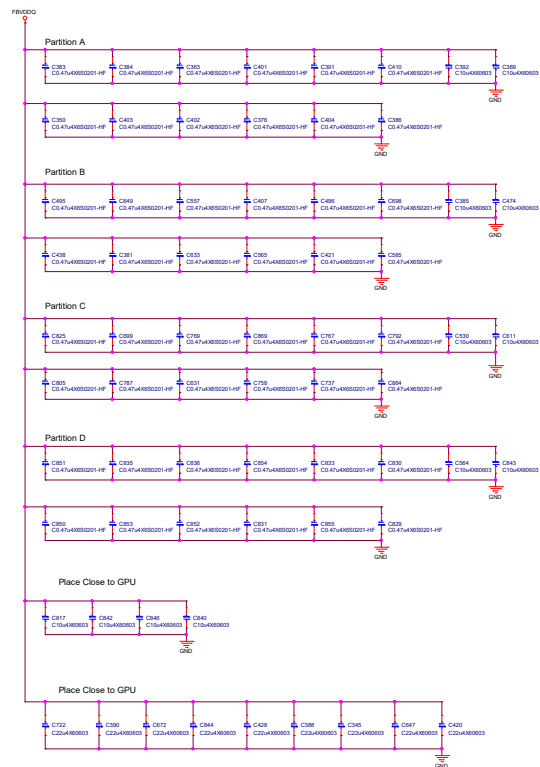
BG45 VDD R23
BG46 VDD R24
BG47 VDD R25
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BG51 VDD R29
BG52 VDD R30
BH44 VDD R31
BH45 VDD R32
BH47 VDD R33
BH48 VDD R34
BH49 VDD R35
BH50 VDD R36
BH51 VDD R37
BH52 VDD R38
BJ44 VDD R39
BJ45 VDD R40
BJ46 VDD T13
BJ47 VDD T40
BJ48 VDD U13
BJ49 VDD U14
BJ50 VDD U15
BJ51 VDD U16
BJ52 VDD U17
BK47 VDD U18
BK48 VDD U19
BK49 VDD U20
BK50 VDD U21
BK51 VDD U22
BK52 VDD U23
BL46 VDD U24
BL47 VDD U25
BL48 VDD U26
BL49 VDD U27
BL50 VDD U28
BL51 VDD U29
BL52 VDD U30
BM47 VDD U31
BM48 VDD U32
BM49 VDD U33
BM50 VDD U34
BM51 VDD U35
N13 VDD U36
N14 VDD U37
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N19 VDD V40
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P13 VDD W34
P40 VDD W35
R13 VDD W36
R14 VDD W37
R15 VDD W38
R16 VDD W39
R17 VDD W40
R18 VDD Y13
R19 VDD Y40
R20 VDD
R21 VDD
R22 VDD

<https://realschematic.com>

Title: GPU PWR AND GND		
Size:	Document Number: CustomMS-16U71 / 17E7	Rev: 0A
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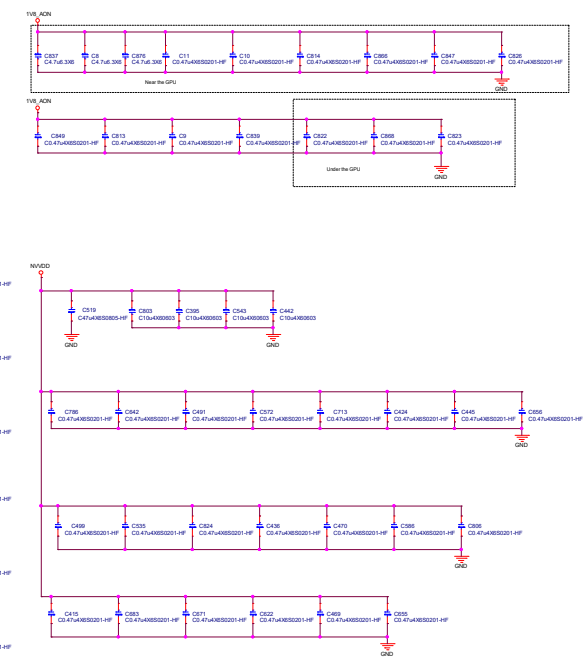
FBVDDQ_GPU



NVVDD

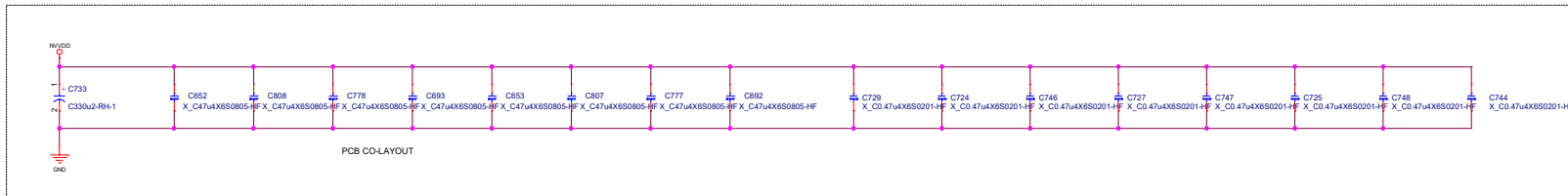
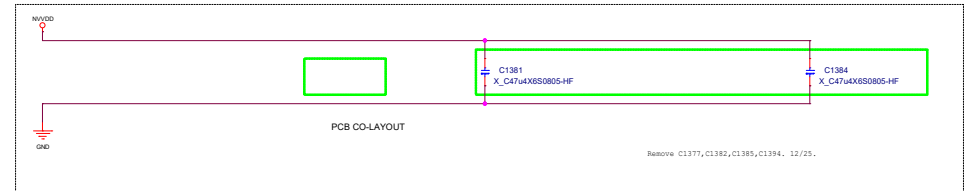
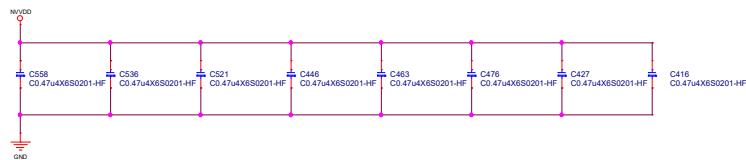
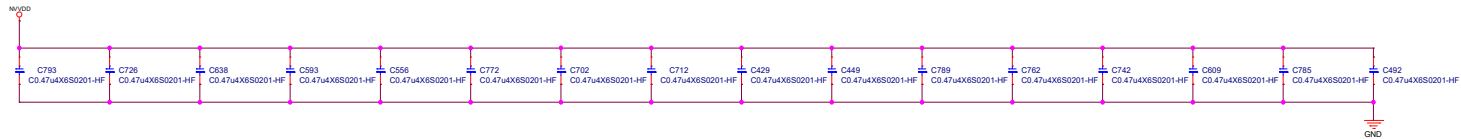
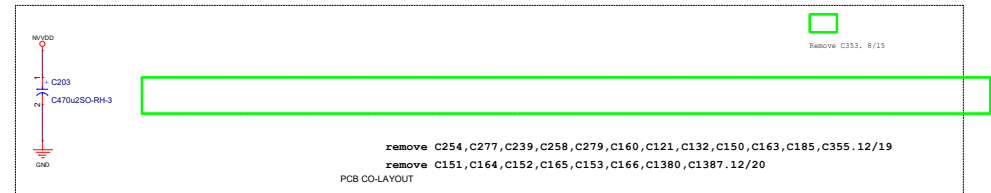
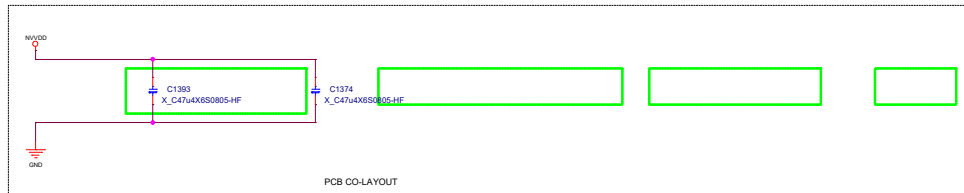
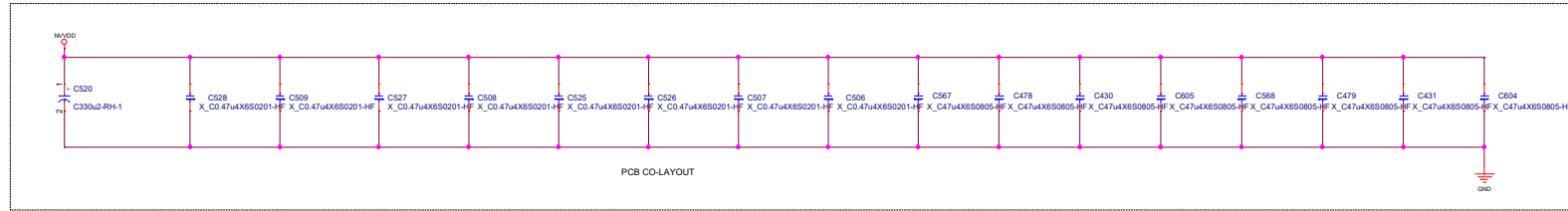


1V8_AON

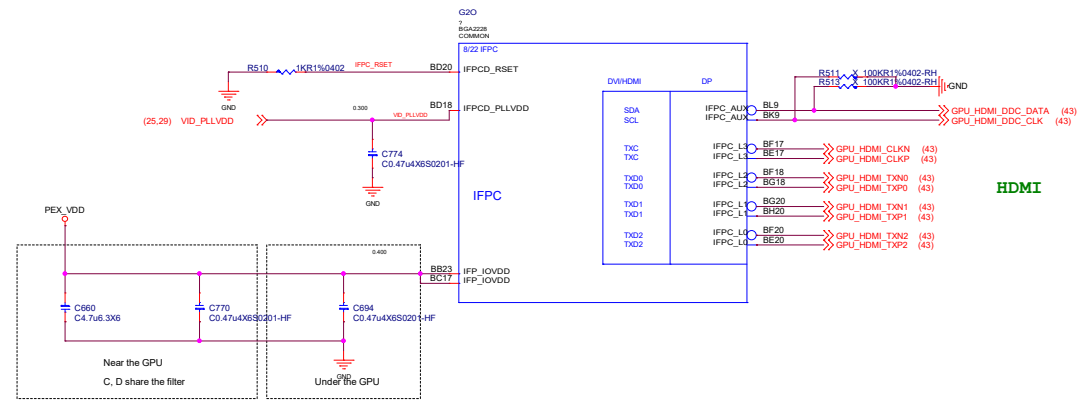
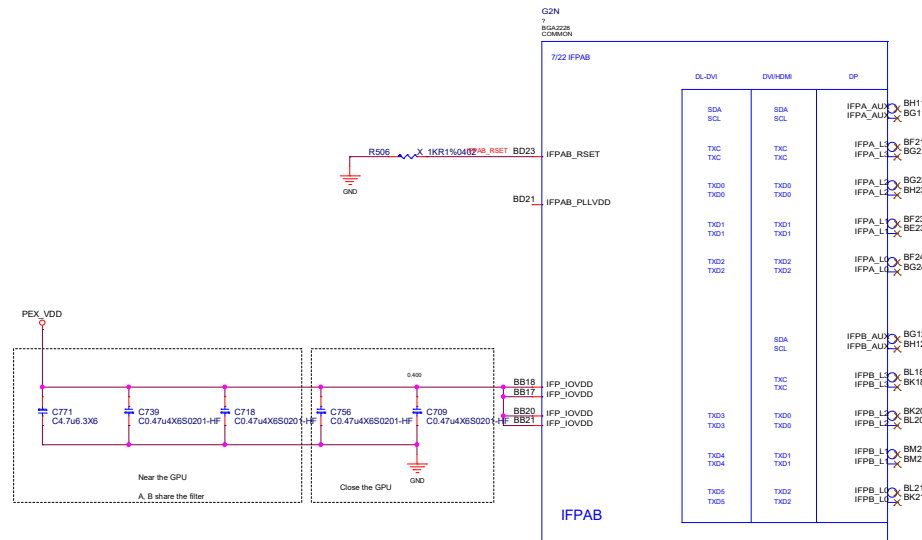


GPU DECOUPLING B

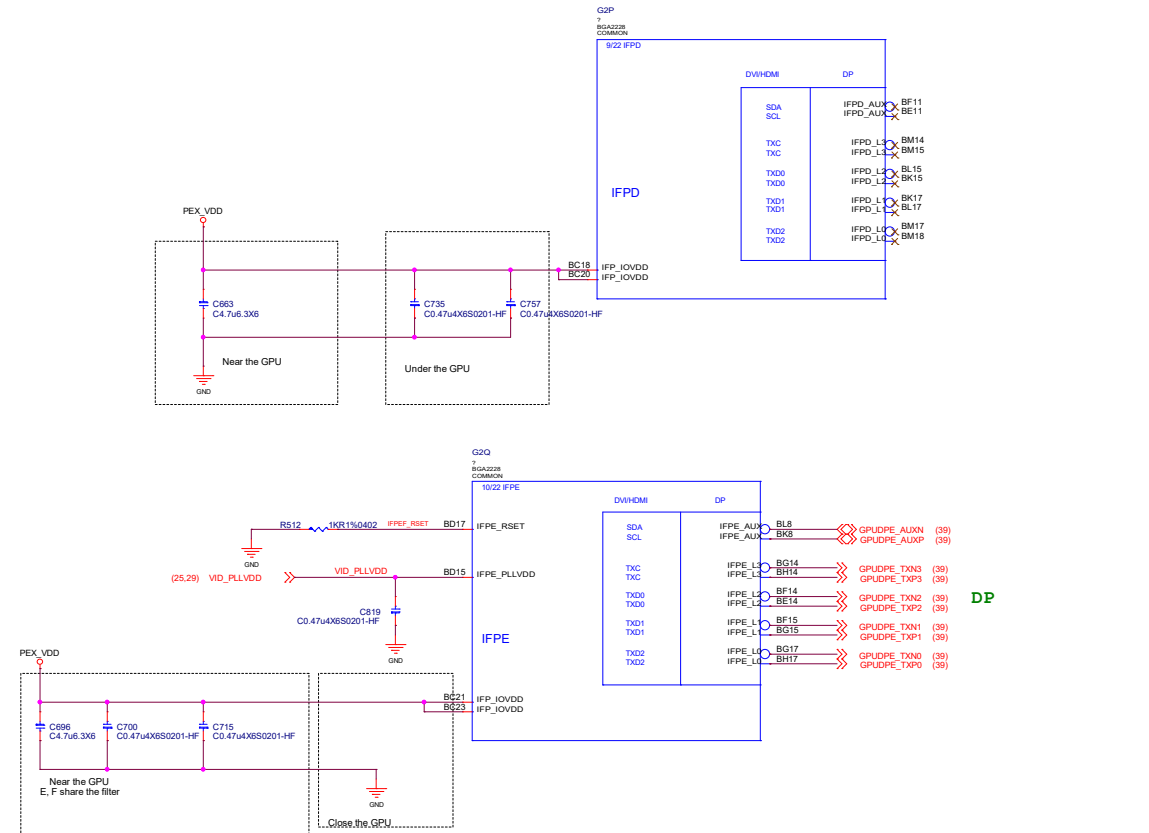
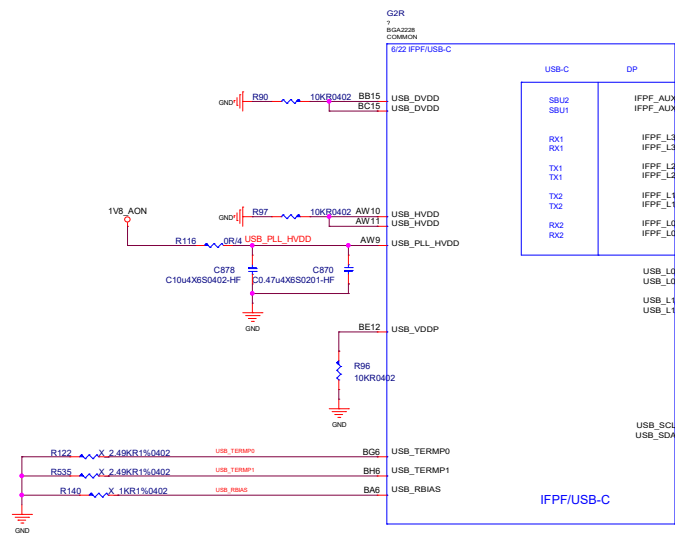
GPU Decoupling



DACA,Display IF

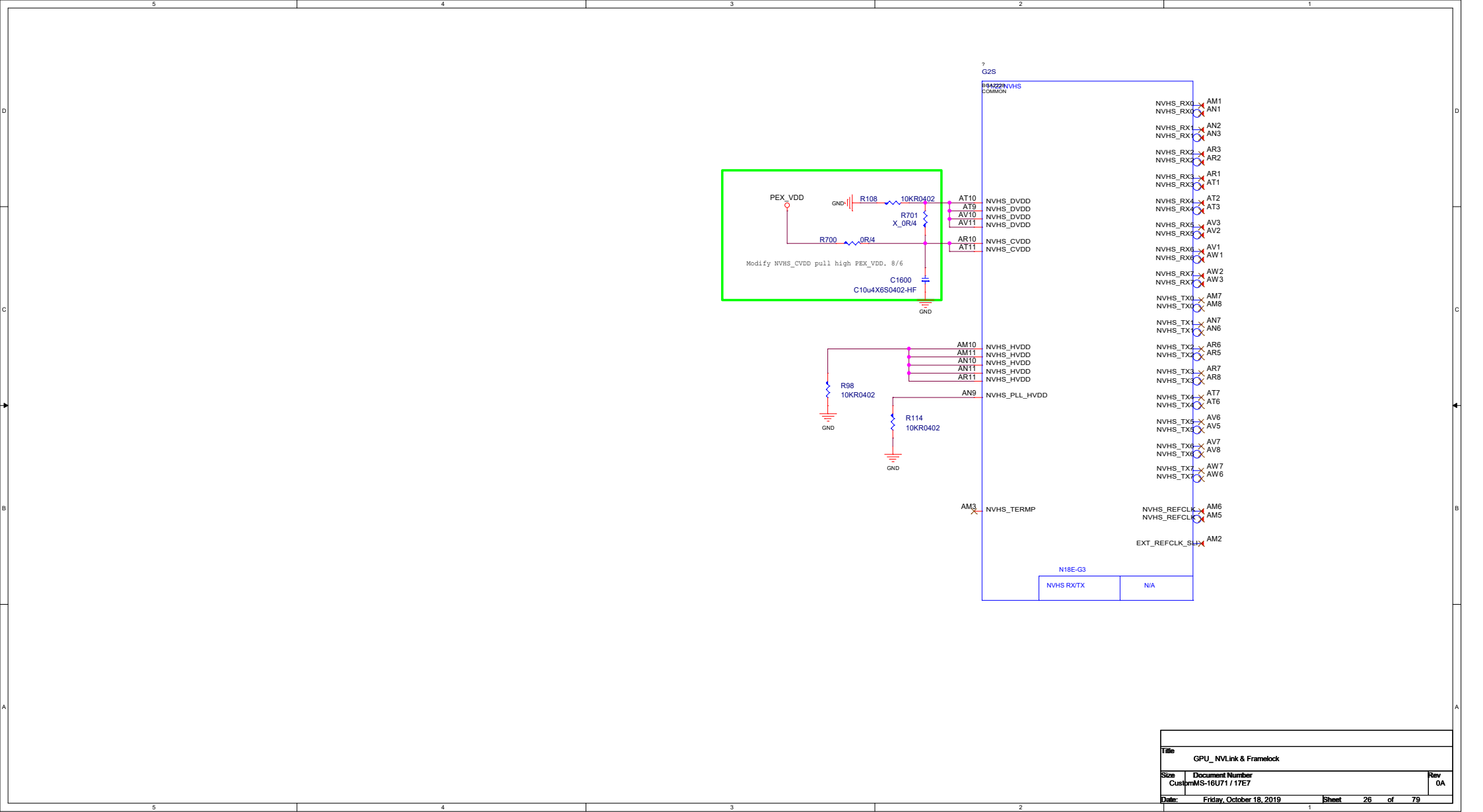


HDMI



DP

<https://realschematic.com>



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG TBD
L	L	H	0001	RAMCFG TBD
L	H	L	0010	RAMCFG TBD
L	H	H	0011	RAMCFG TBD
H	H	L	0110	RAMCFG TBD
H	H	H	0111	RAMCFG TBD

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

[illegible]

1V8 AON

PCI_DEVID

R175
X_100KR1%0402-RH

R168
X_100KR1%0402-RH

R166
X_100KR1%0402-RH

ROM SI

ROM SO

ROM SCLK

R177
100KR1%0402-RH

R167
10KR1%0402

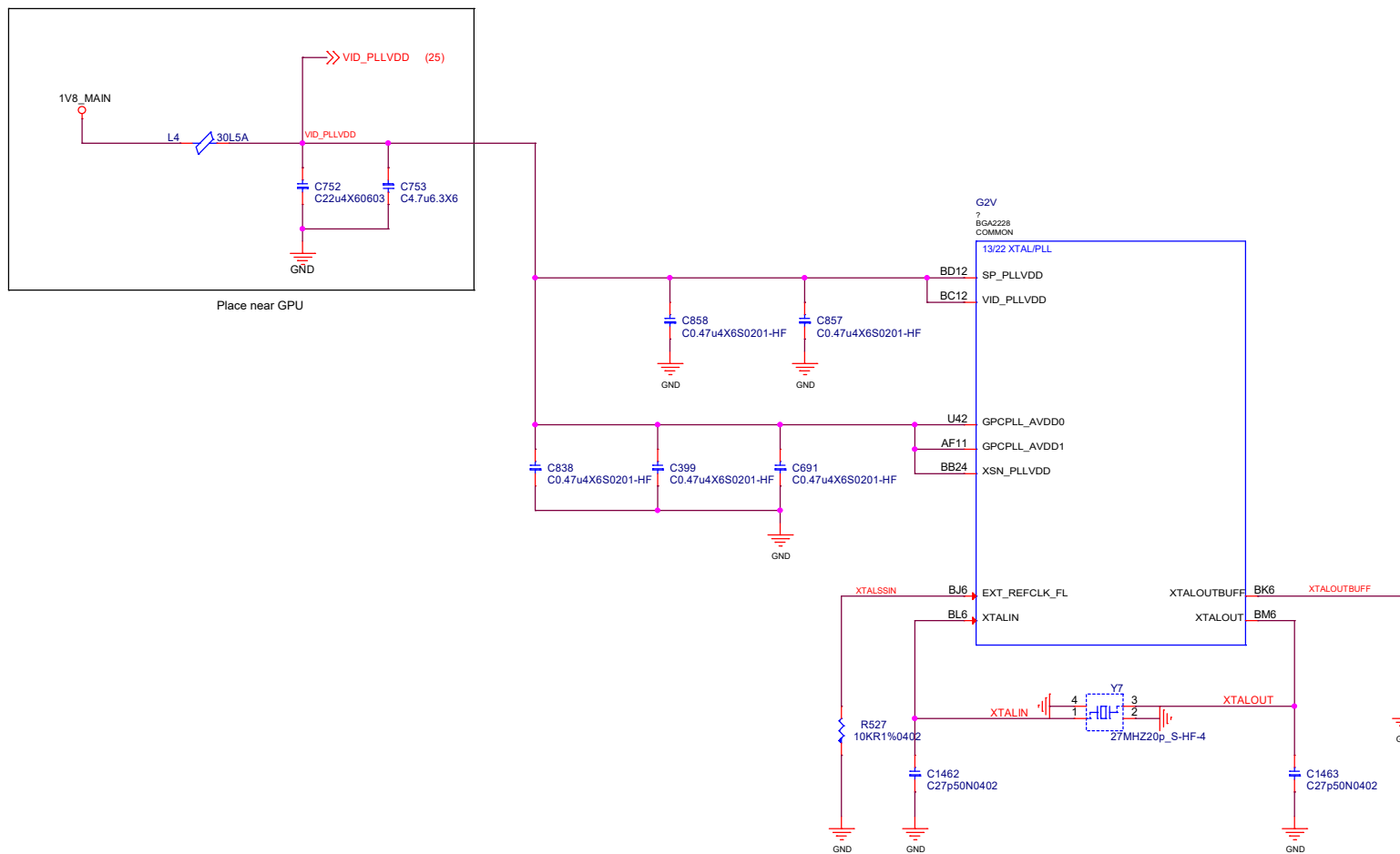
R165
100KR1%0402-RH

GND

GND

GND





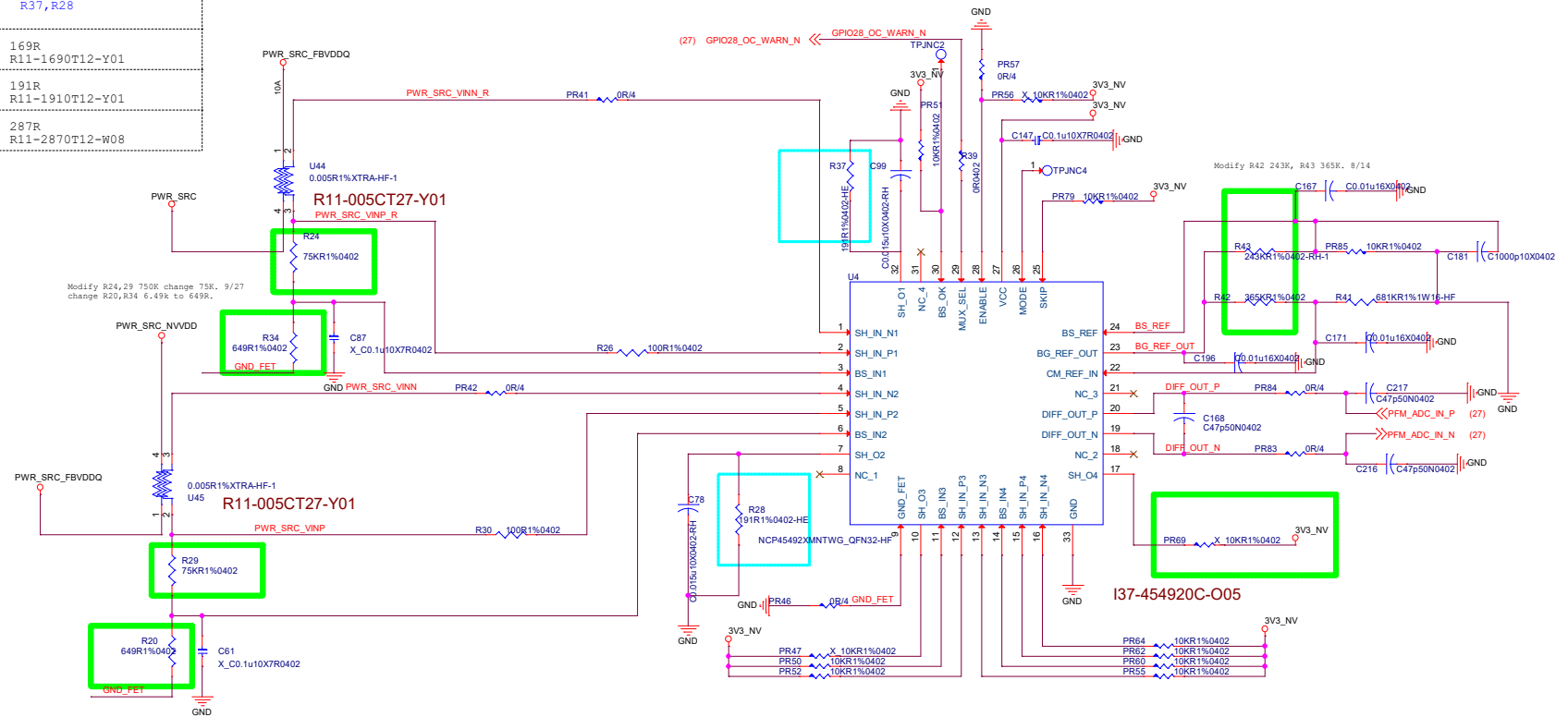
Place near GPU

SmartFan Strap Table

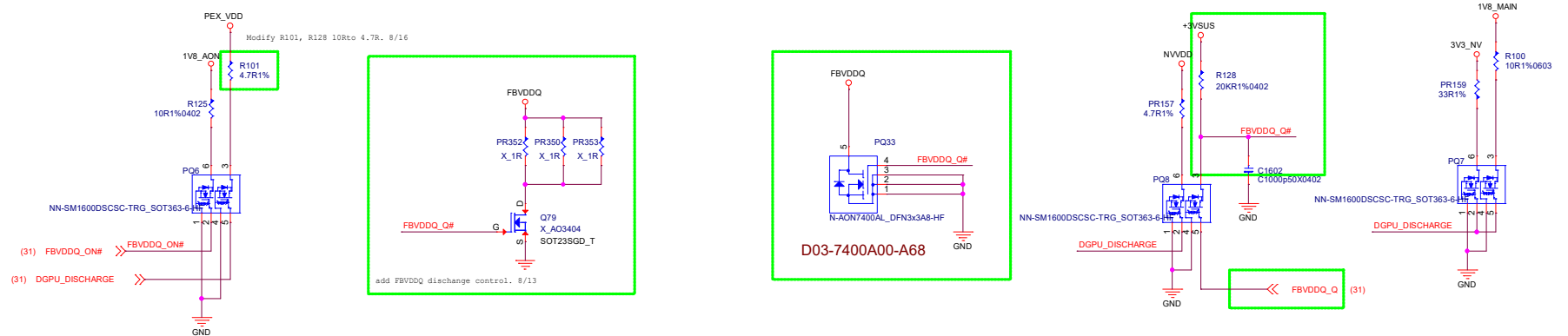
XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM

DGPU_Power Control

TGP	SKU	R24, R29	R34, R20	C87, C61 先不上件	R37, R28
150W	G3	75K	649R	1nF	169R R11-1690T12-Y01
115W	G2	75K	649R	1nF	191R R11-1910T12-Y01
80W	G1/G0	75K	649R	1nF	287R R11-2870T12-W08

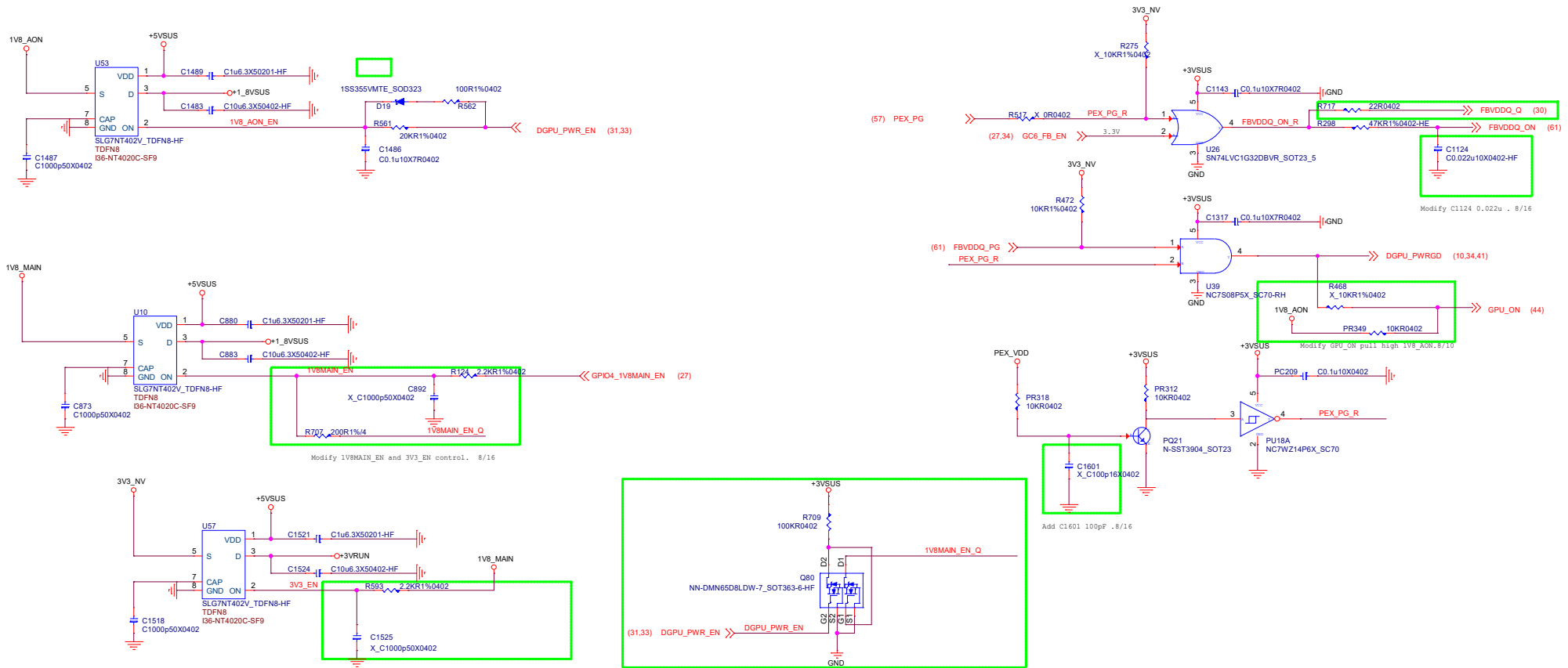


Discharge



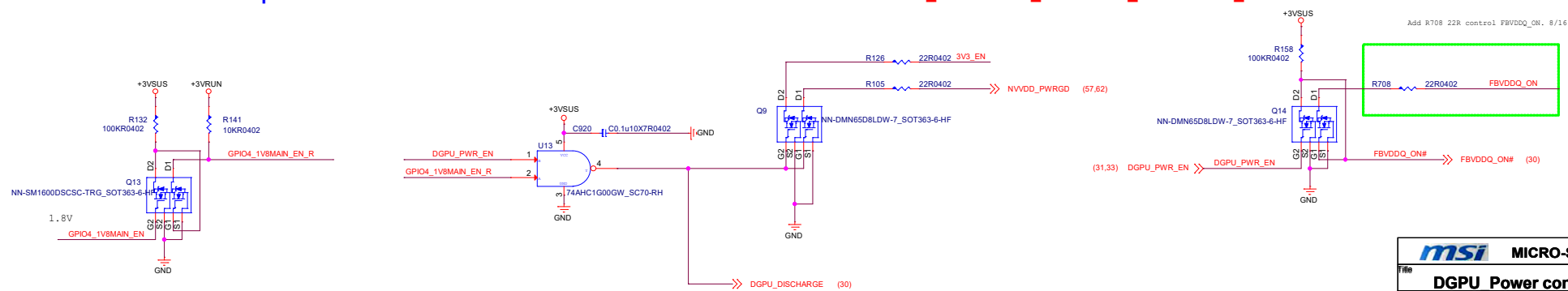
nVIDIA Power Sequence Power UP

Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD



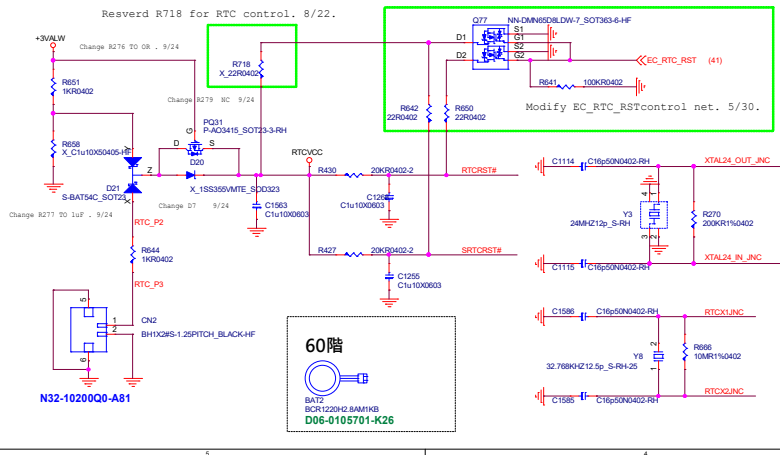
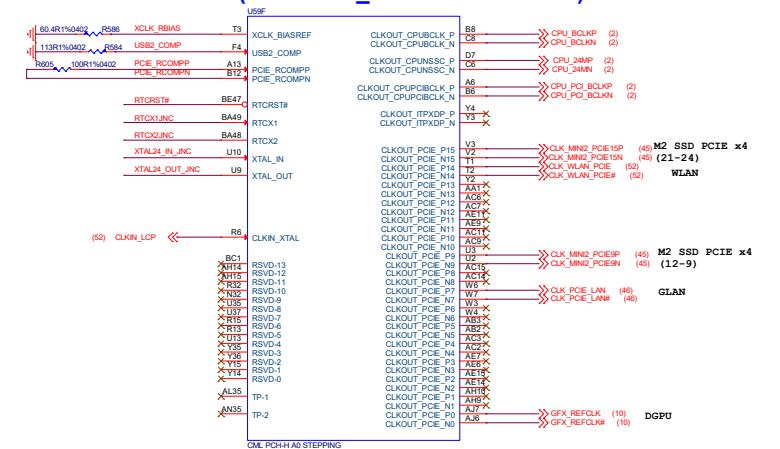
nVIDIA Power Sequence Power Down

Power down = FBVDDQ -> NVDDS/PEX_VDD -> 3V3_NV -> 1V8_AON -> 1V8_MAIN

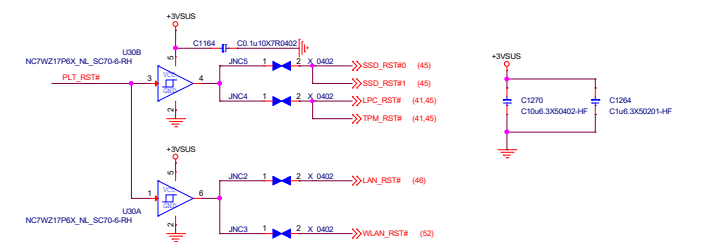
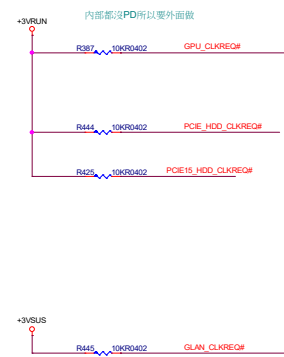
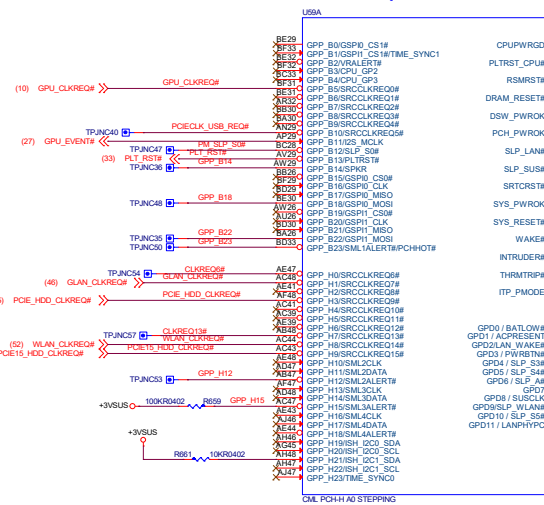


msi MICRO-STAR INT'L CO.,LTD.	
File	DGPU Power control, Discharge
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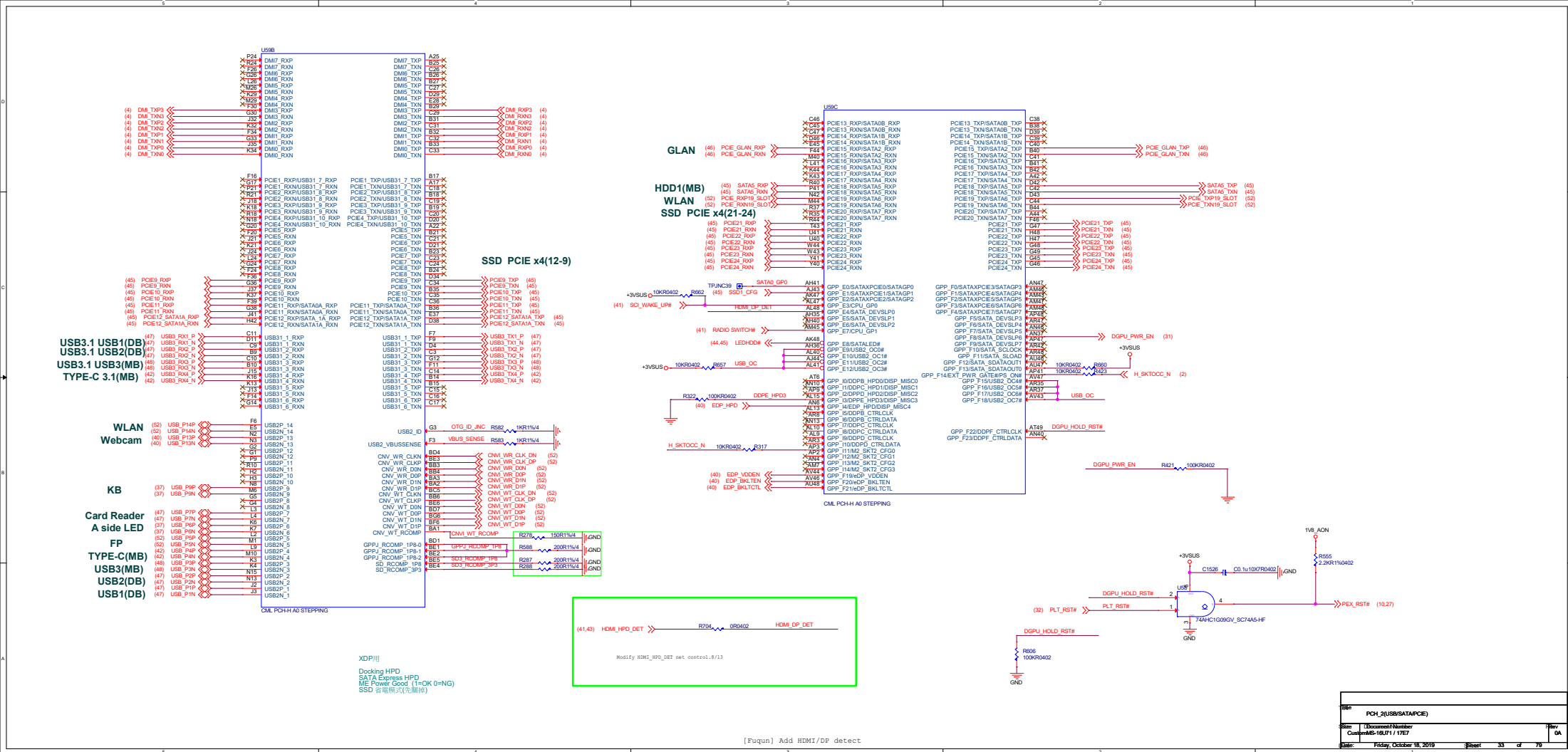
HM370 (RTC/PCIE_Clock/Clock/RSVD)



HM370 (CLKREQ/ACPI)



Title			
PGH_1(CLK/DDI)			
Size	Document Number	Rev	
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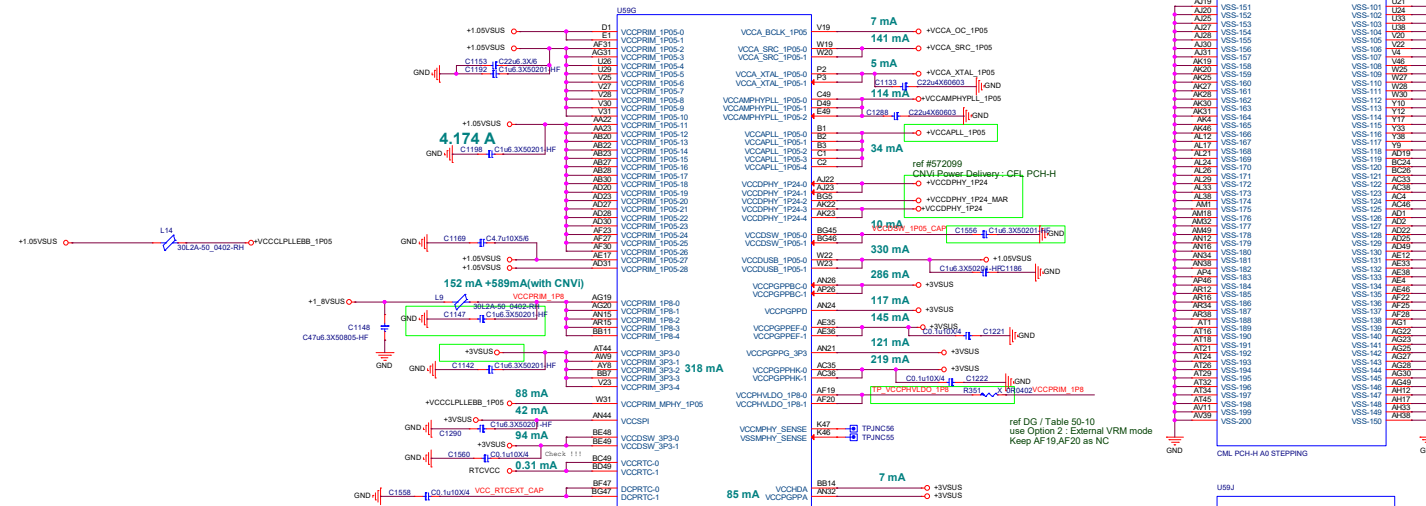


PCH EDS Page 52



HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



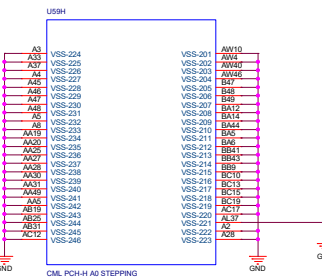
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCGPPBC	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCGPPF	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCGPPG_3P3	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCGPPH	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCGPPK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCGPPJ	1.8V or 3.3V
Primary Well Group J (GPP_J)	VCCGPPK	1.8V or 3.3V
Primary Well Group K (GPP_K)	VCCGPPK	1.8V or 3.3V
Primary Well Group L (GPP_L)	VCCGPPK	1.8V or 3.3V
Primary Well Group M (GPP_M)	VCCGPPK	1.8V or 3.3V
Primary Well Group N (GPP_N)	VCCGPPK	1.8V or 3.3V
Primary Well Group O (GPP_O)	VCCGPPK	1.8V or 3.3V
Primary Well Group P (GPP_P)	VCCGPPK	1.8V or 3.3V
Primary Well Group Q (GPP_Q)	VCCGPPK	1.8V or 3.3V
Primary Well Group R (GPP_R)	VCCGPPK	1.8V or 3.3V
Primary Well Group S (GPP_S)	VCCGPPK	1.8V or 3.3V
Primary Well Group T (GPP_T)	VCCGPPK	1.8V or 3.3V
Primary Well Group U (GPP_U)	VCCGPPK	1.8V or 3.3V
Primary Well Group V (GPP_V)	VCCGPPK	1.8V or 3.3V
Primary Well Group W (GPP_W)	VCCGPPK	1.8V or 3.3V
Primary Well Group X (GPP_X)	VCCGPPK	1.8V or 3.3V
Primary Well Group Y (GPP_Y)	VCCGPPK	1.8V or 3.3V
Primary Well Group Z (GPP_Z)	VCCGPPK	1.8V or 3.3V

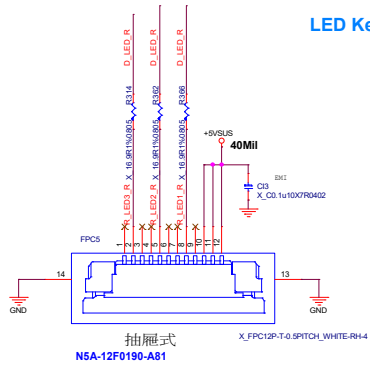
Note: Except for GPP_U group, the operating voltage of a GPIO group having voltage configurability (1.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage selection self-strap to the desired voltage. GPP_C group voltage is selected by setting the corresponding self-strap only.

Power Descriptions for PCH in CNL-H

Name	Description
VCCA_BCLK_1P0S	Analog supply for BCLK circuitries: 1.05V
VCCA_SRC_1P0S	Analog supply for PCIe clock circuitries: 1.05V
VCCA_XTAL_1P0S	Analog supply for XTAL circuitries: 1.05V
VCCDUSB_1P0S	Supply for USB digital logic: 1.05V
VCCAPLL_1P0S	Analog supply for BCLK/DMI/Audio PLLs: 1.05V. This rail can be derived from the VCCPRIM_1P0S rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P0S	Primary Well: 1.05V. For PCIe/USB3/SATA MPHY logic, I/O blocks, SRAM, ITAG, CNVI.
VCCDSW_1P0S	Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P0S	Mod PHY Primary: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB6 PLL dividers
VCCAMPHYPLL_1P0S	Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P0S	1.8V Primary Well.
VCCPRIM_3P3	3.3V Primary Well.
VCCSP1	SP1 Primary Well 3.3V or 1.8V, for SPI interface.
VCCD0A	HDA Audio Power 3.3V, 1.8V, or 1.5V, for Intel® High Definition Audio.
VCCDSW_3P3	3.3V Deep Sx Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained.
VCCDPHY_1P24	1.24V for CNVI logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVLDIO_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPRIM_1P0 rail in Internal 1.8V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCGPPA	1.8V or 3.3V for GPP_A group.
VCCGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCGPPD	1.8V or 3.3V for GPP_D group.
VCCGPPF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCGPPG_3P3	3.3V for GPP_G group.
VCCGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
V5SMPHY_SENSE	0V (Ground) Sense Line.
V5S	Ground.



Doc	PCH_S(Power1)	Rev	0A
Doc	Document Number		
Doc	Compartments: B071 / 117		
Date	Friday, October 18, 2019	Printed	36 of 79

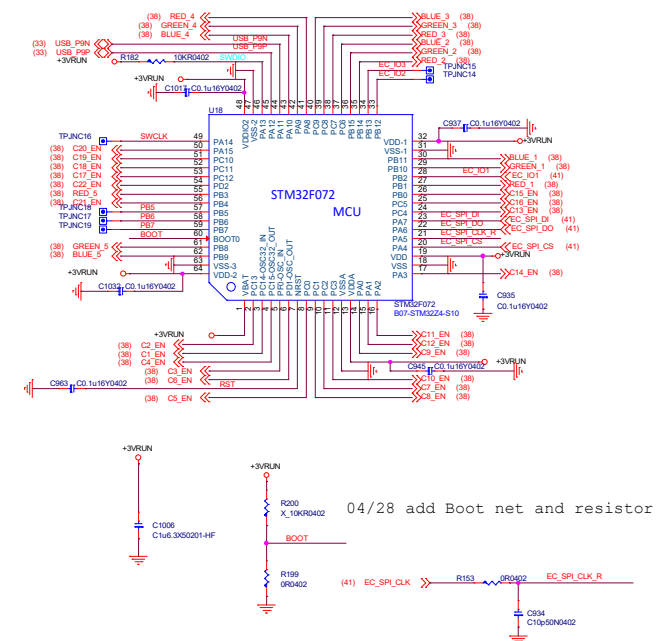


LED Keyboard CONN

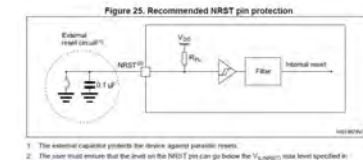
LED Keyboard Pin Define	RED LED Keyboard Pin Define
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

(41) LED1_EN >> Q78
X_AO3404
SOT23BGD_T
For RED LED Keyboard control. 8/4

LED STM32F072 Controller

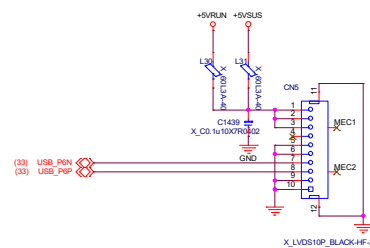


04/28 add Boot net and resistor



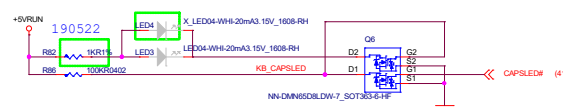
1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the V_{IL} reset level specified in Table 10. NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

A side LED



GE	CN5 use
GP/GL/WE	CN5 no use

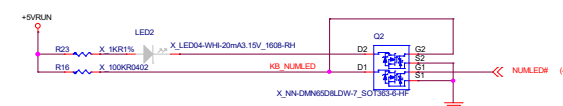
CAPSLED Add LED4 for17"



	LED3, LED4
GE	D0C-040C300-L05
GP	D0C-0402010-L05

	LED3
17E1/17E2	D0C-040C300-L05

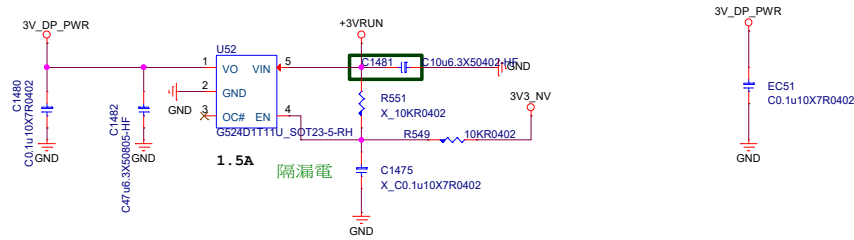
NUMLED



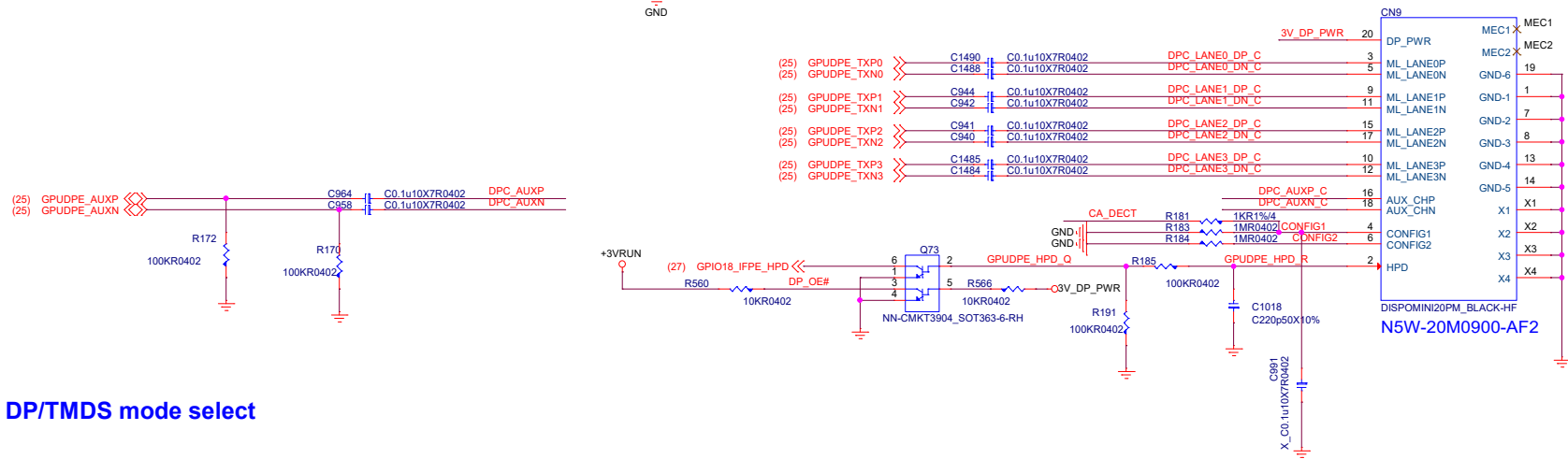
File	LED 805/KB CON
Rev	1
Customer Number	17E1 / 17E2
Date	Friday, October 18, 2019
Sheet	37 of 79

Display Port

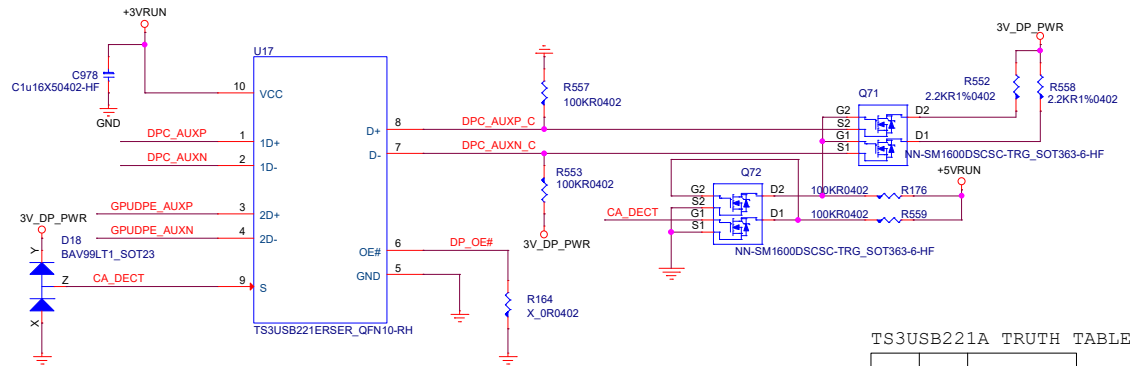
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



Display Port



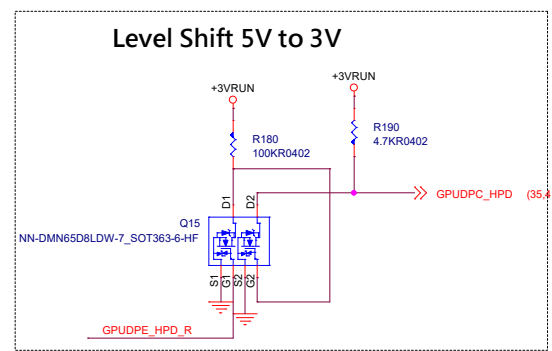
DP/TMDS mode select



TS3USB221A TRUTH TABLE

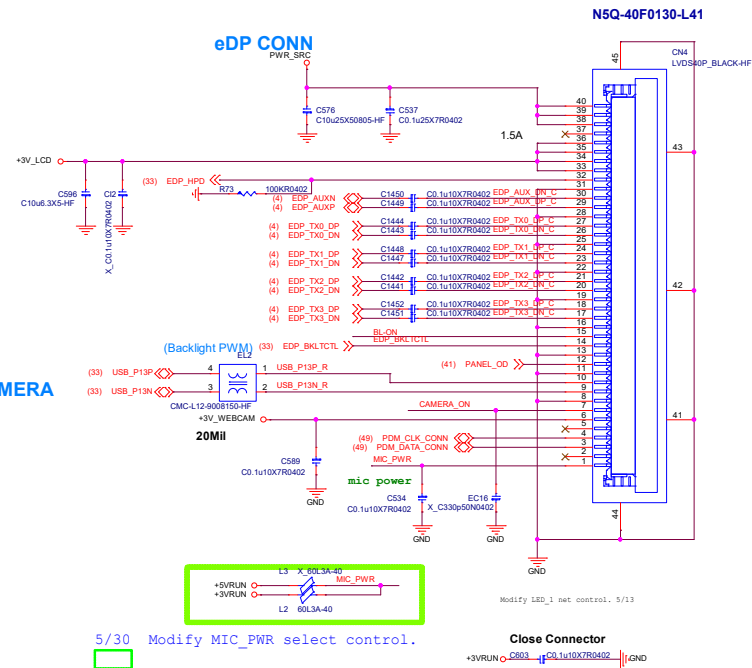
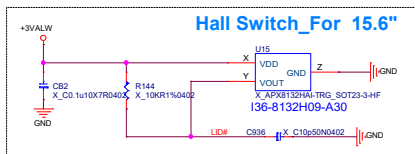
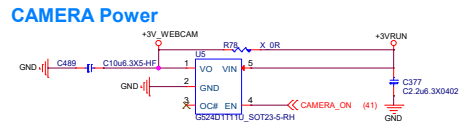
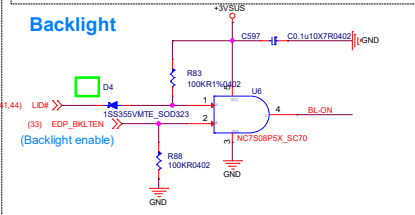
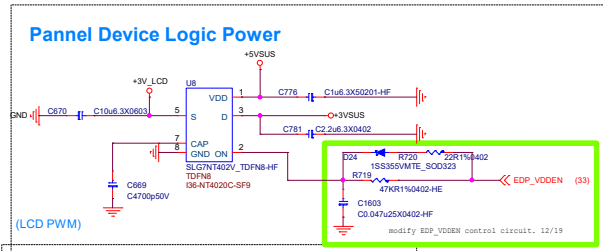
S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

Level Shift 5V to 3V



<https://realschematic.com>

eDP/Camera



LCD Module Pin Define FOR FULL HD PANEL

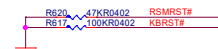
Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	OD_EN	OD_Enable Signal of TCON

LCD Module Pin Define FOR WQHD PANEL

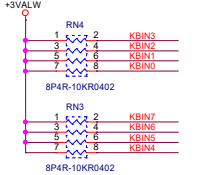
Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	OD_EN	OD_Enable Signal of TCON

KBC/EC/uP (ENE9028)

PU/PD



KB pull Hi 10k



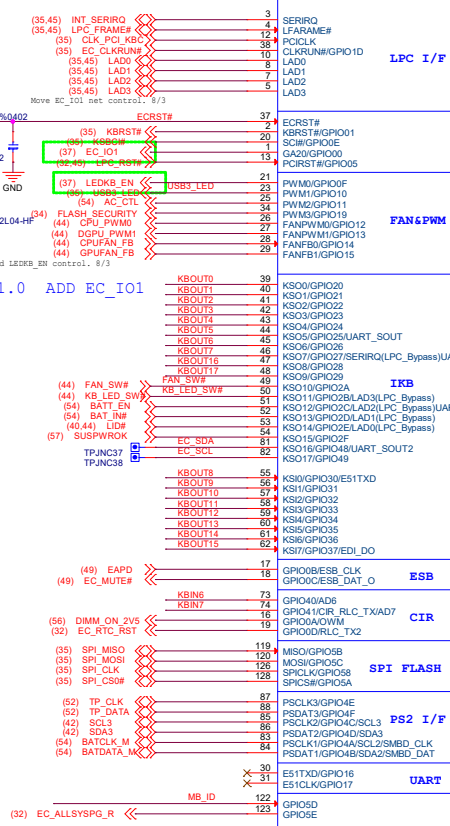
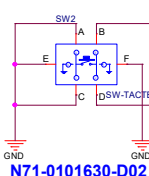
+3VALW LID pull hi 10K



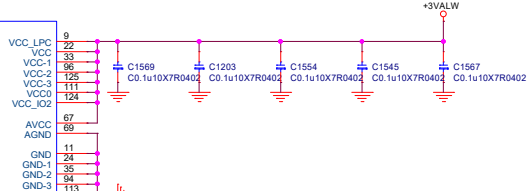
+3VALW



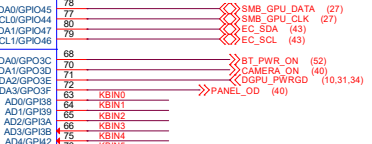
Hardware Reset



POWER/GROUND



SMBUS IEDI



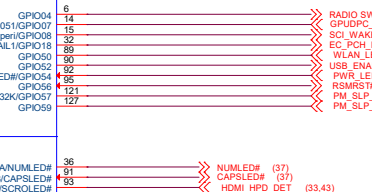
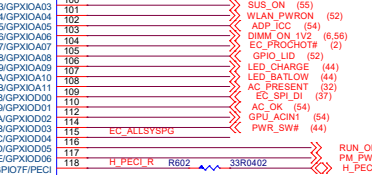
AD/DA



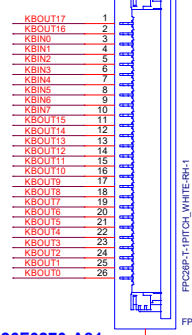
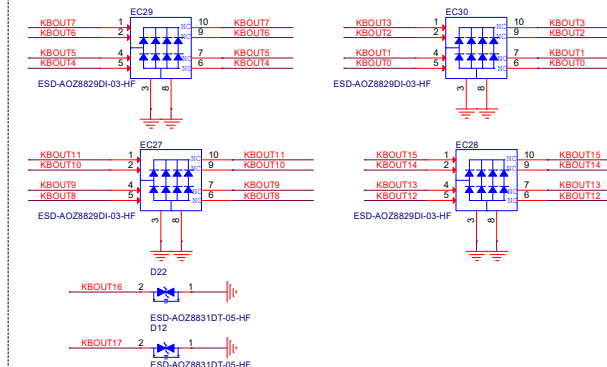
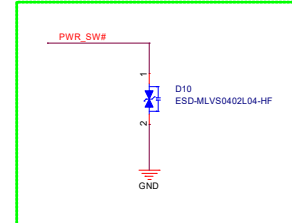
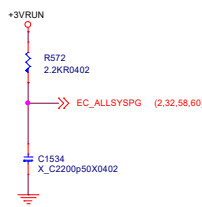
SDI



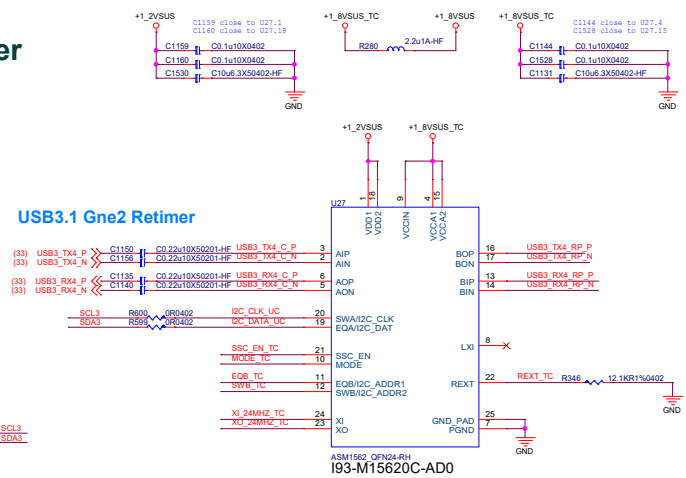
POWER_FAIL0



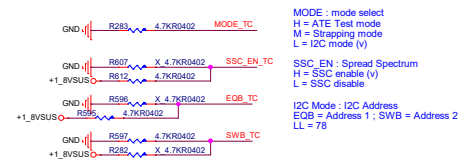
LED



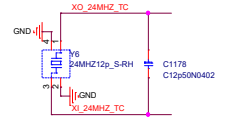
USB3.1 TYPE C
ASM1562 Re-timer



Strap

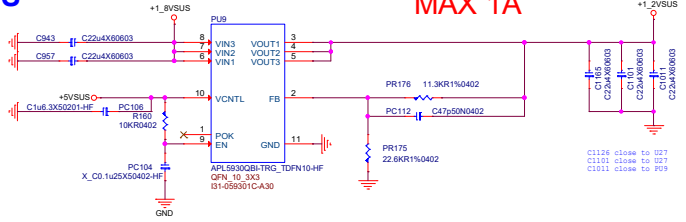


24MHz Clock

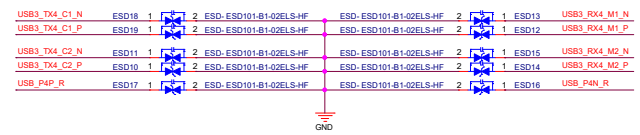


+1_2VSUS

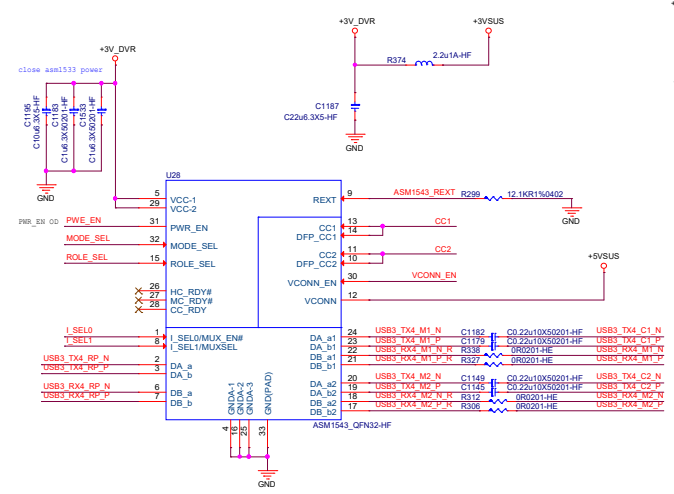
MAX 1A



ESD



ASM1543 Mux with CCL



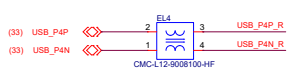
Function Table

Pin	Signal	Mode	Level
R365	10KR0402	I_SELO	1.5V
R300	10KR0402	I_SEL1	1.5V

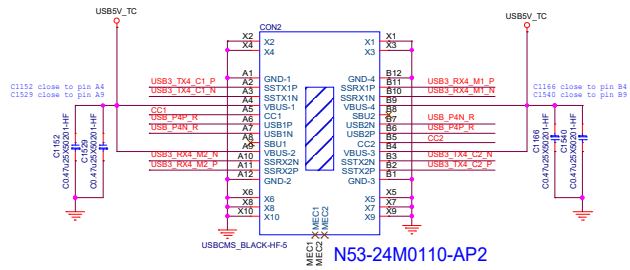
Strapping Table

Pin	Signal	Mode	Level
R365	2.2KR0402	MODE_SEL	1.5V
R295	2.2KR0402	ROLE_SEL	1.5V
R365	2.2KR0402	VCONN_EN	1.5V

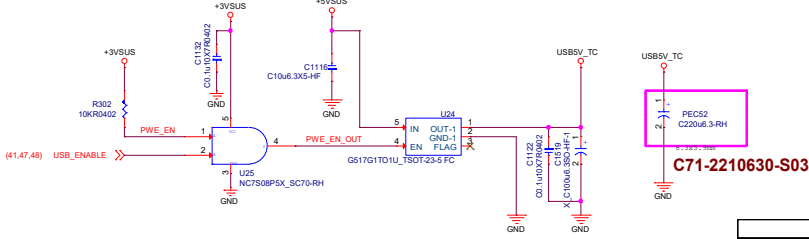
USB20 CMC



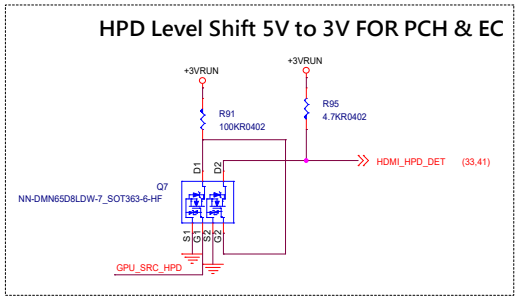
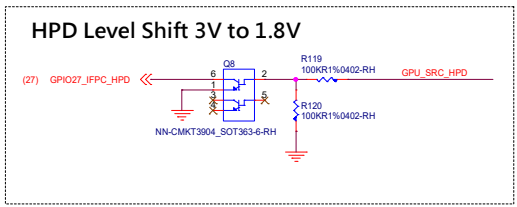
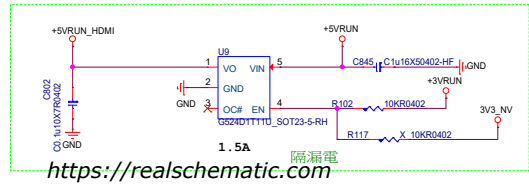
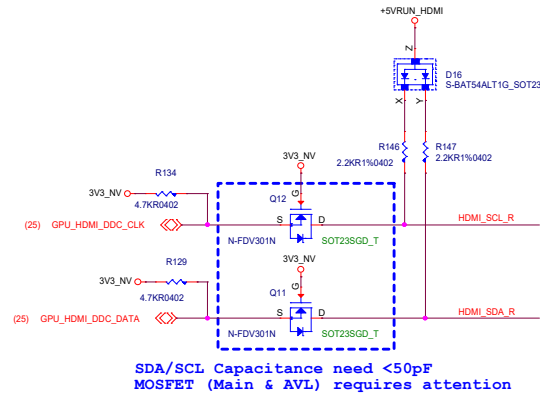
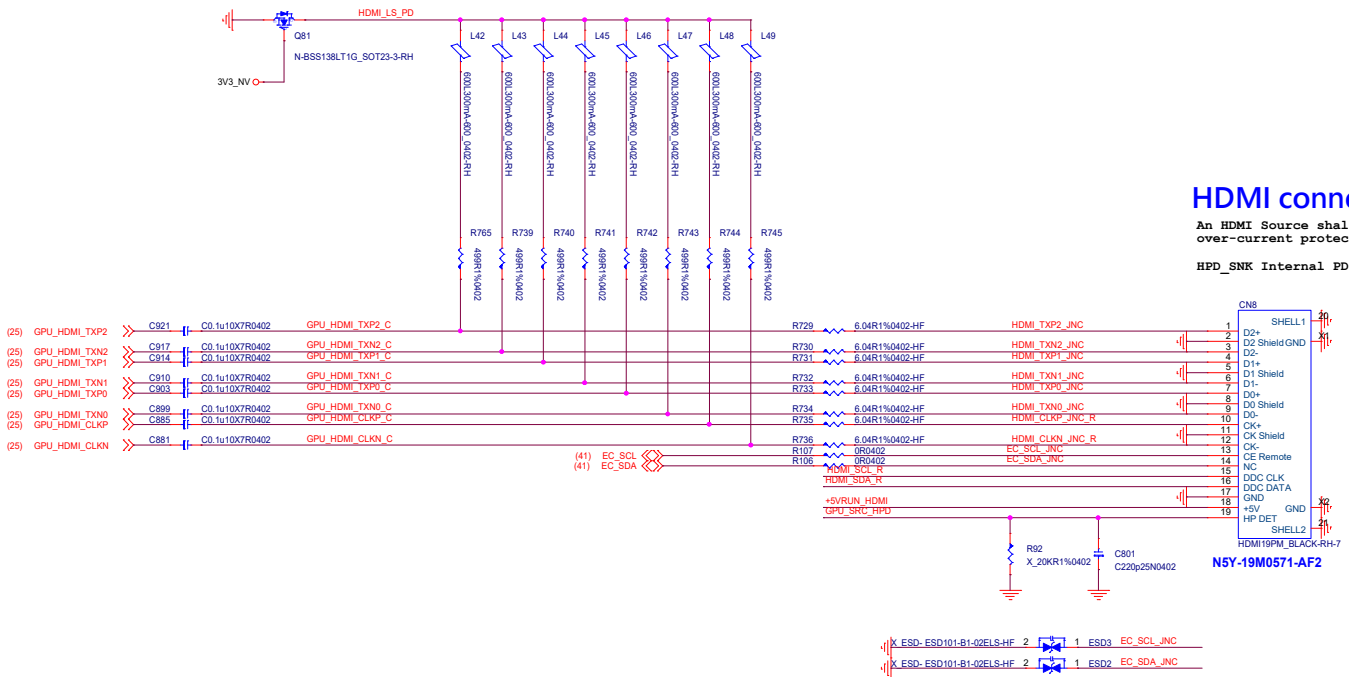
Type-C Connector



PWR Switch

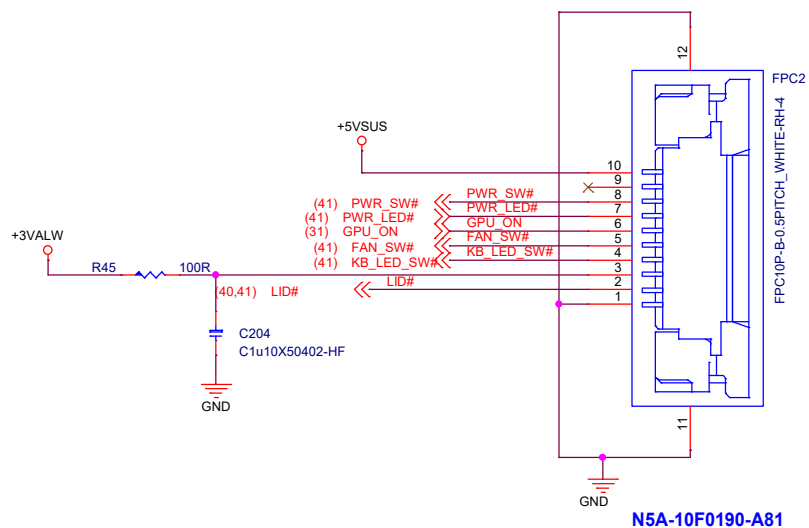


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Size	100KB
Version	1.0
Date	Friday, October 18, 2019
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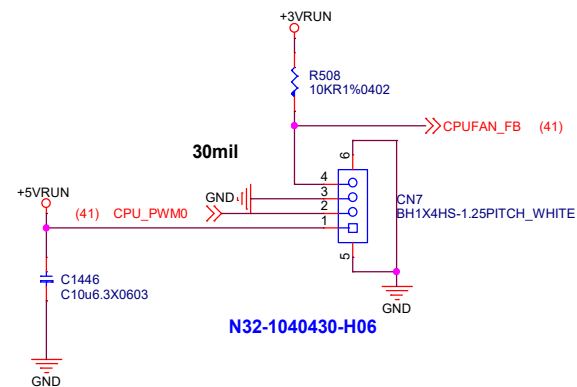


CPU FAN/CPU FAN/POWER CONN/ LED CONN

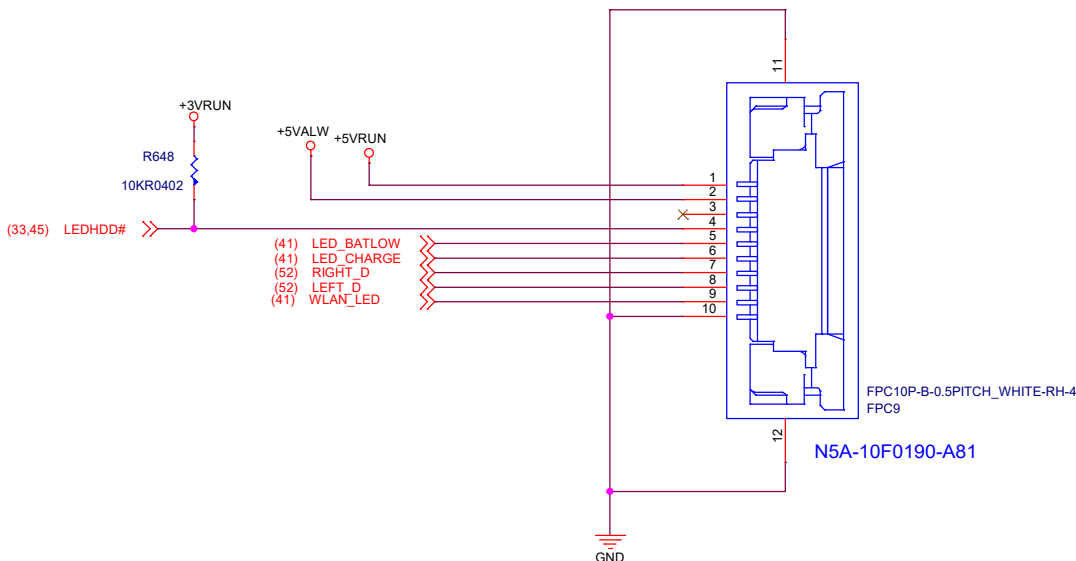
Power Switch Connector



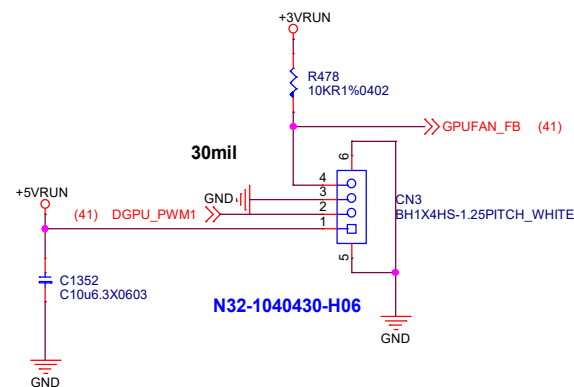
CPU FAN



Switch connector

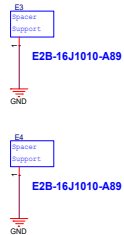


DGPU FAN

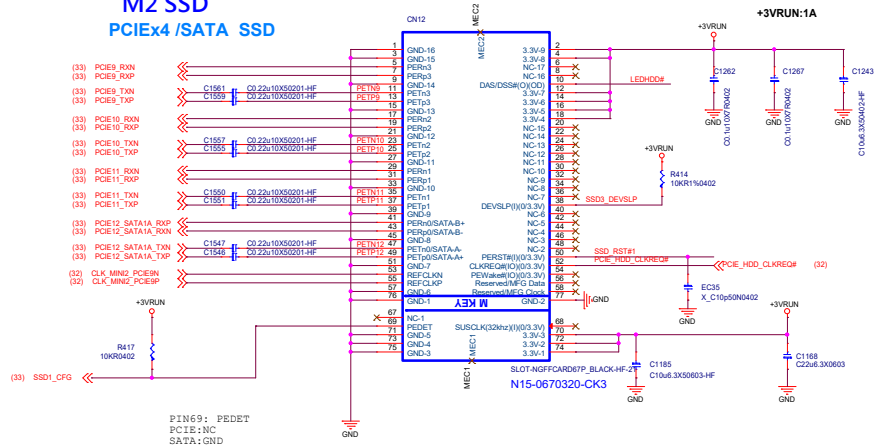


msi MICRO-STAR INT'L CO.,LTD.	
Title	
CPU FAN/BTB CONN/LED	
Size	Document Number
Custom	MS-16U71 / 17E7
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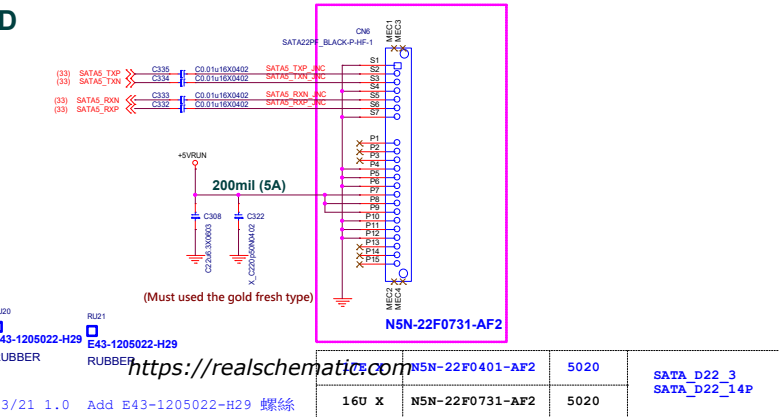
PCIEx4



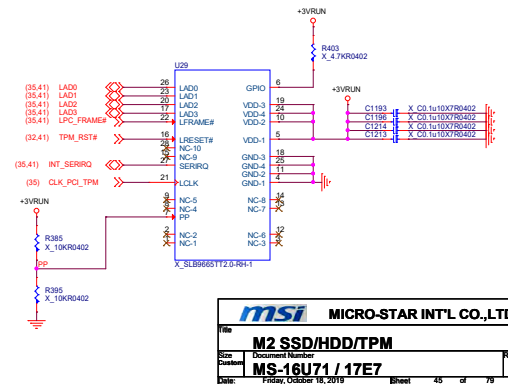
M2 SSD
PCIEx4 /SATA SSD



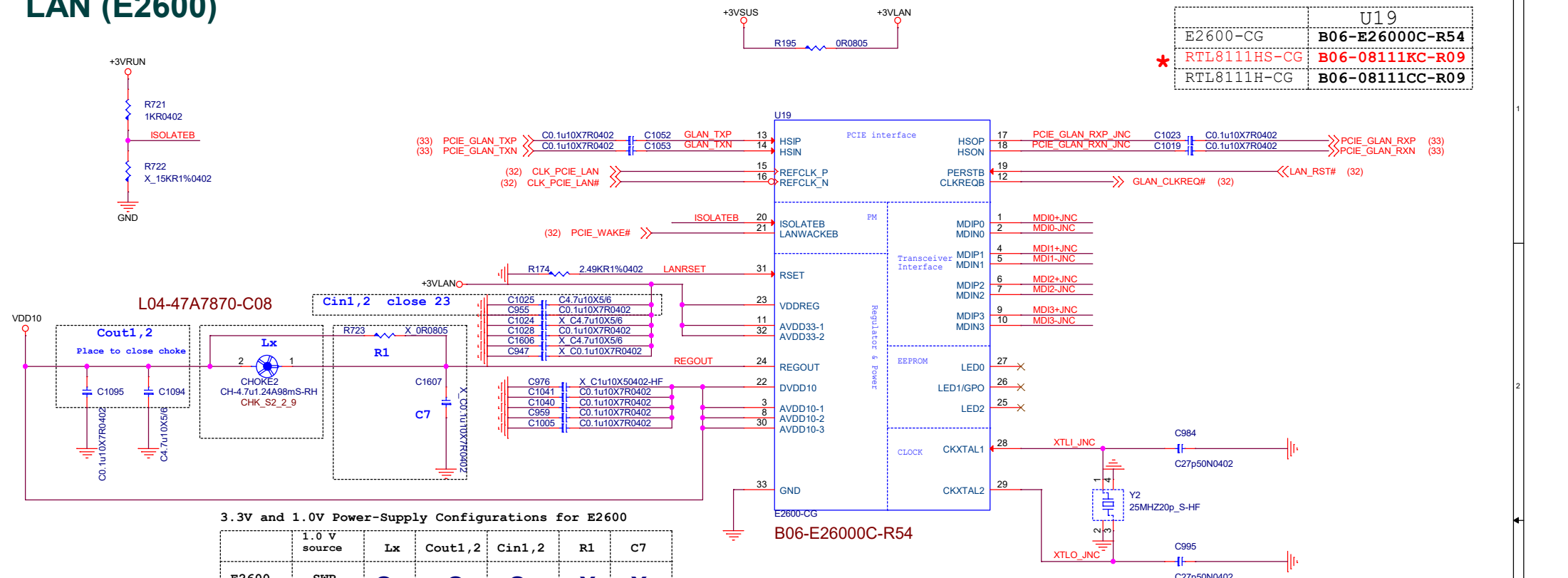
HDD



TPM

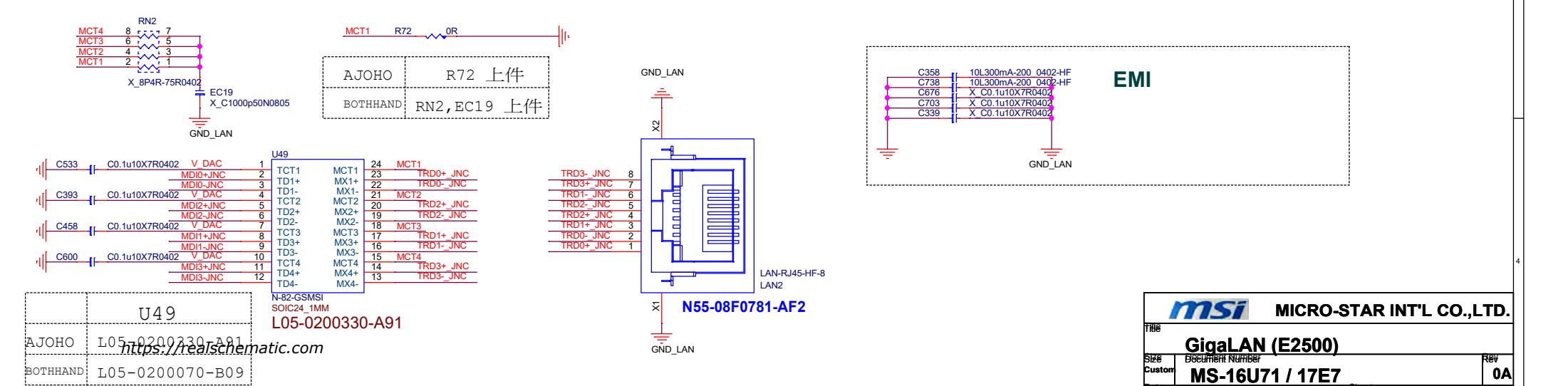


LAN (E2600)

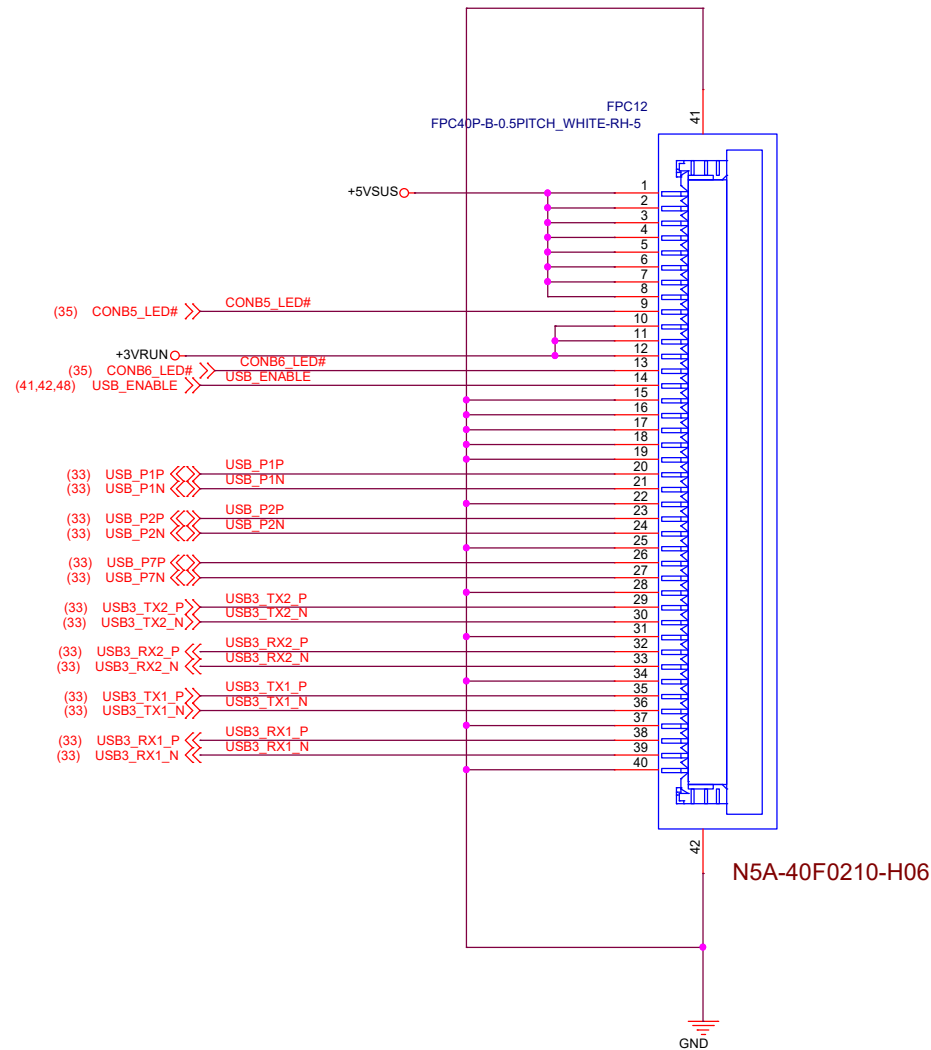


3.3V and 1.0V Power-Supply Configurations for E2600

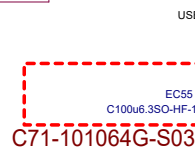
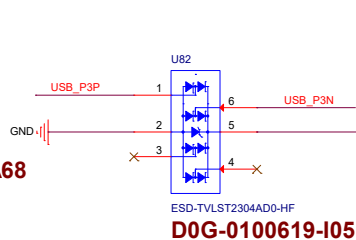
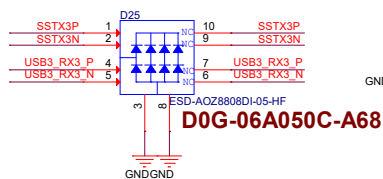
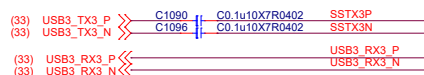
	1.0 V source	Lx	Cout1,2	Cin1,2	R1	C7
E2600	SWR	O	O	O	X	X
RTL-8111HS	SWR	O	O	O	X	X
RTL-8111H	Regout	X	X	X	O	O



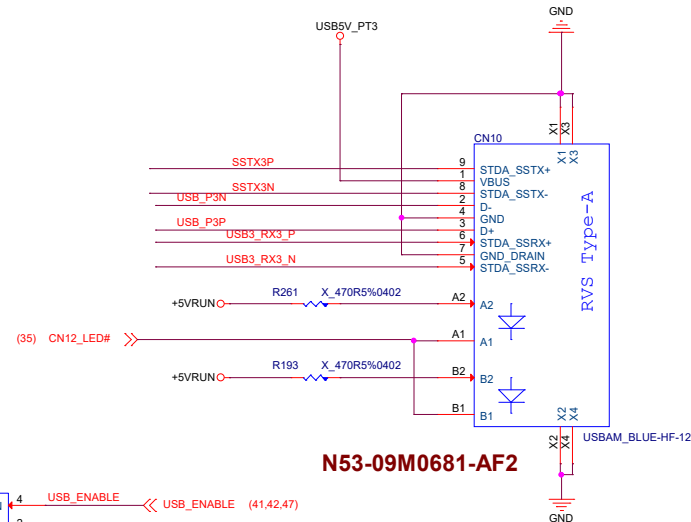
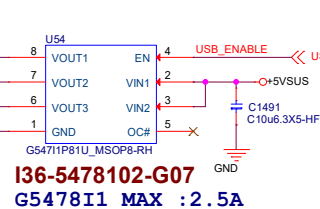
E2600-CG	B06-E26000C-R54
RTL8111HS-CG	B06-08111KC-R09
RTL8111H-CG	B06-08111CC-R09



msi MICRO-STAR INT'L CO.,LTD.	
Title	
B to B connector	
Size	Document Number
Custom	MS-16U71 / 17E7
Date:	Friday, October 18, 2019
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Rev	0A

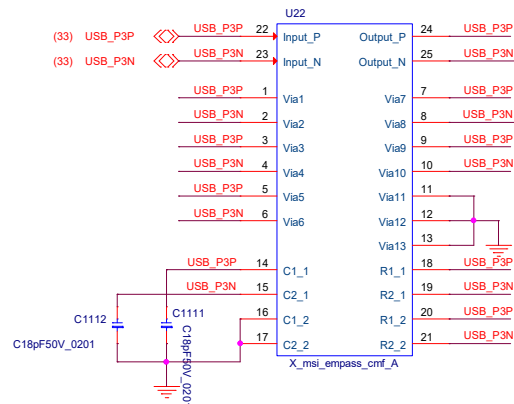
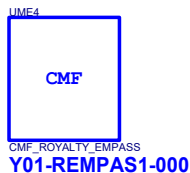


20190605 Change
for inrush current

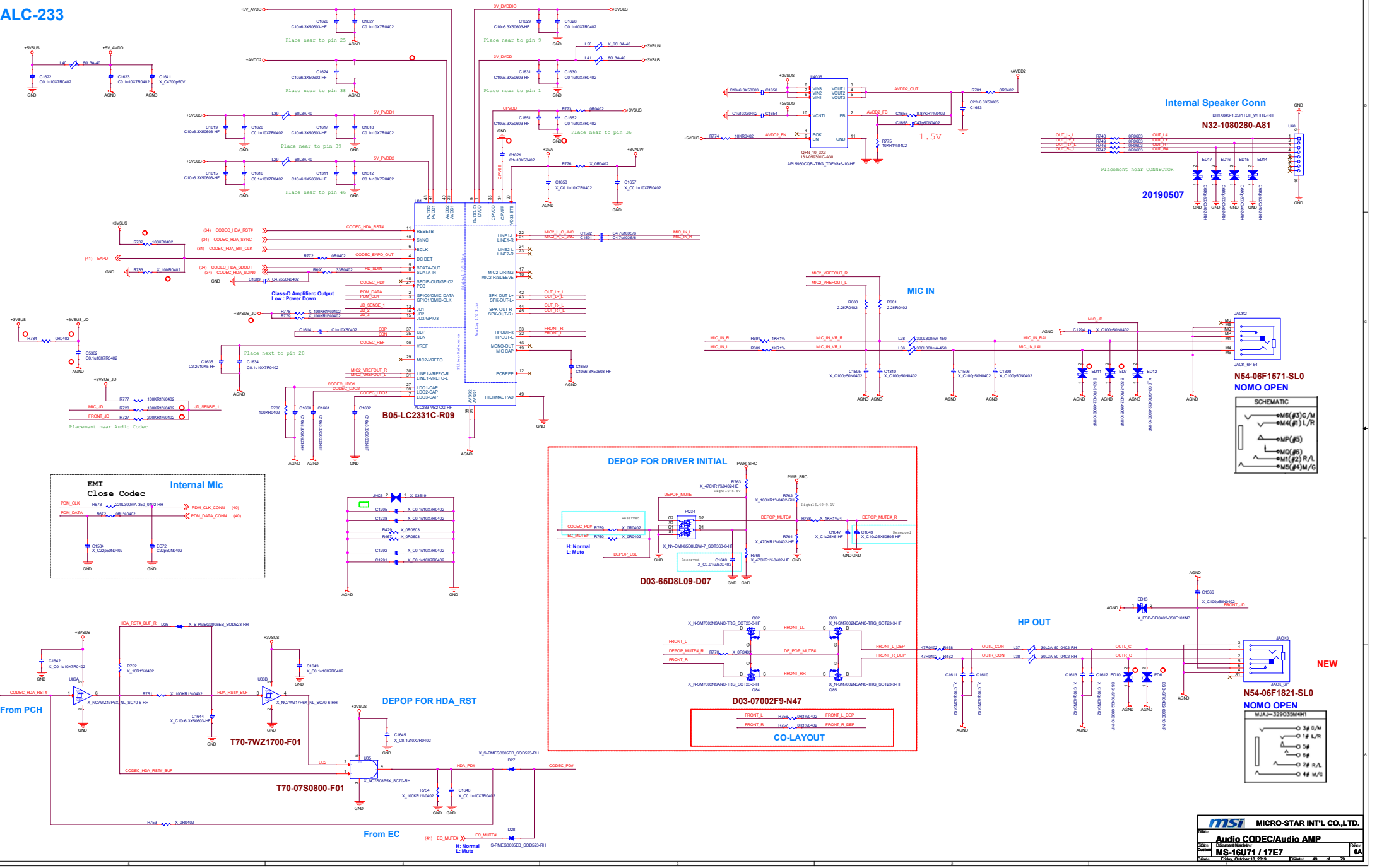



USB3.0_LED 60	N53-13M0031-L06	USB_A1_13_USB3_0P
USB3.0 50X0	N53-09M0681-AF2	Co-layout use
USB3.1_GEN2 50X0	N53-09M1021-AF2	USB_A1_13_USB3_0_1P
USB3.1_GEN2_LED 60	N53-13M0041-L06	USB_A1_13_USB3_0_1P

GE	N53-13M0041-L06
GP/GL/WE	N53-09M1021-AF2



msi MICRO-STAR INT'L CO.,LTD.	
USB 3.1 connector	
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		MICRO-STAR INT'L CO.,LTD.	
Title			
Speaker			
Size	Document Number		Rev
C	MS-16U71 / 17E7		0A
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Voltage = 1.8V
Current = 4A
OCP(Min) = 7A



OCP 13A
MAX 10A



Voltage = 1.0V
Current = 3A
OCP (Min) = 7A



TIME	+1.05VSUS/+PEX_VDD/+1_8VSUS
------	------------------------------------

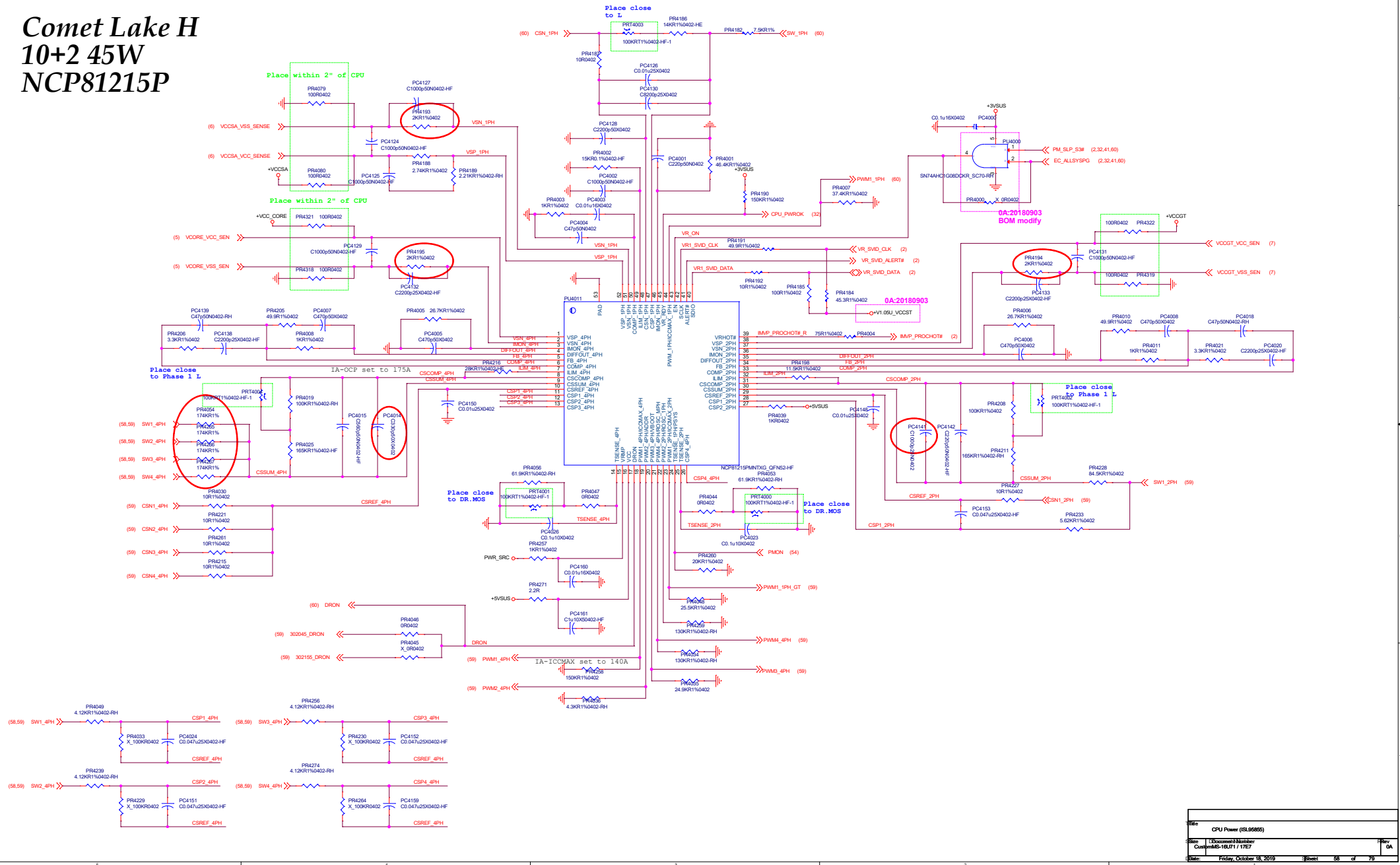
Size Custom Document Number
MS 161171 / 17E7

MS-16071 / 17E7
Date: Friday, October 18, 2019 Sheet 57 of 79

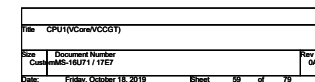
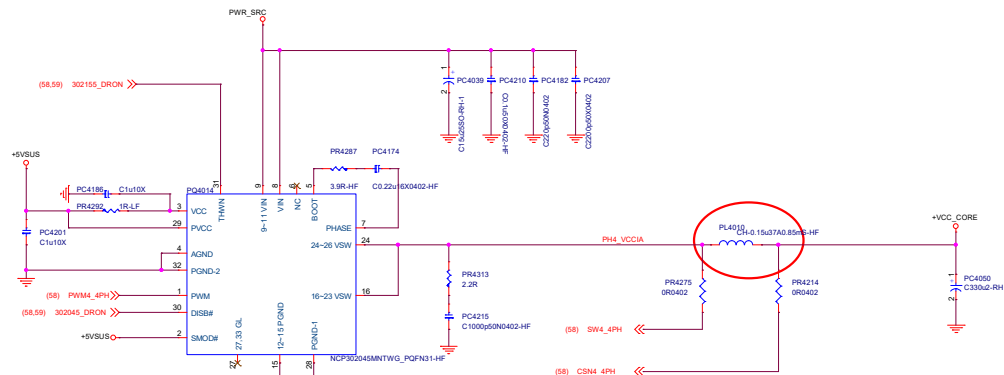
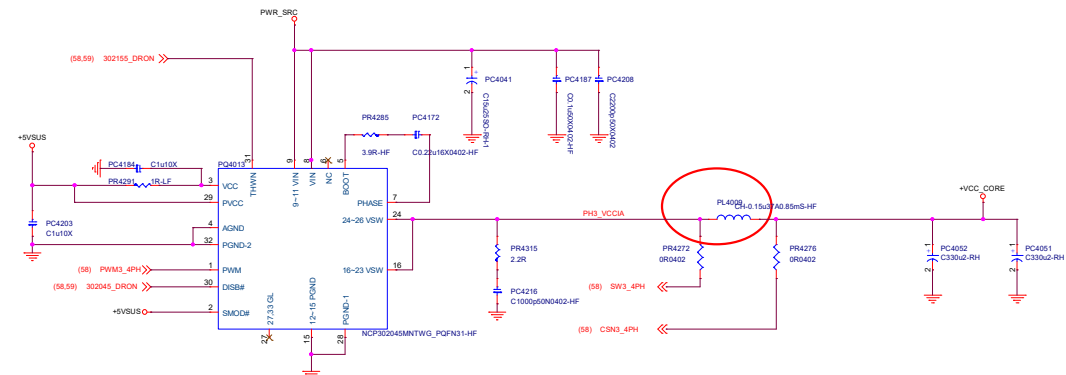
Comet Lake H

10+2 45W

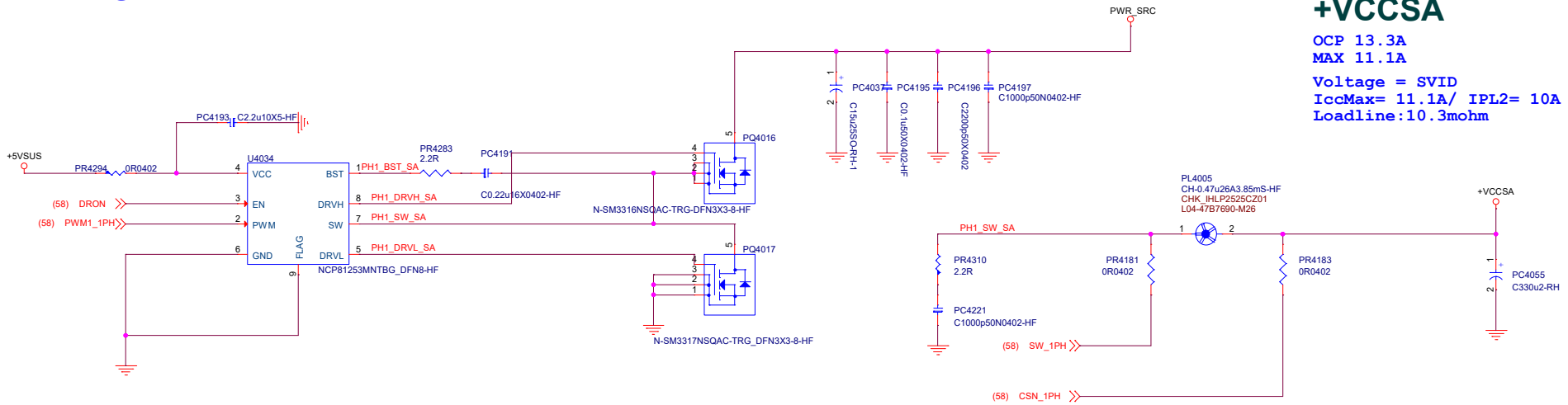
NCP81215P



Rev	CPU Power (SL9686)	Rev	0A
Doc	Document Number	Doc	MS-10171 / 17E7
Date	Friday, October 15, 2019	Sheet	58 of 79

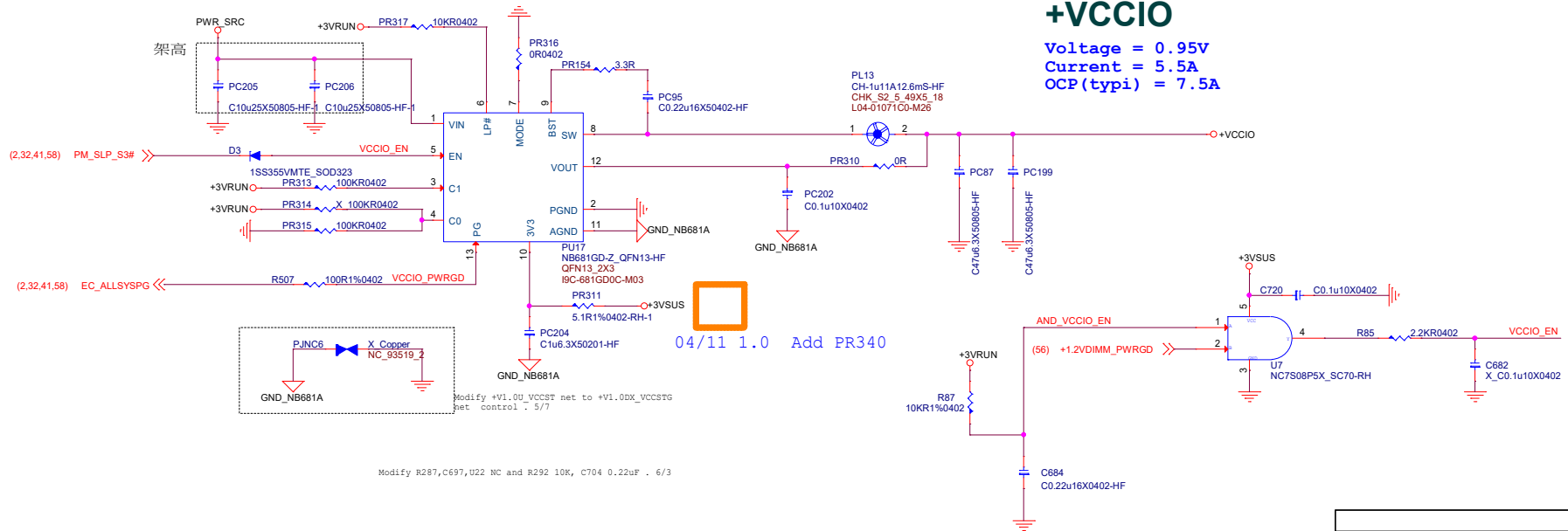


+VCCSA



+VCCIO

Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A



Title				
CPU2(VCCSA/VCCIO)				
Size	Document Number			Rev
Custom	MS-16U71 / 17E7			0A
Date:	Friday, October 18, 2019		Sheet	60 of 79

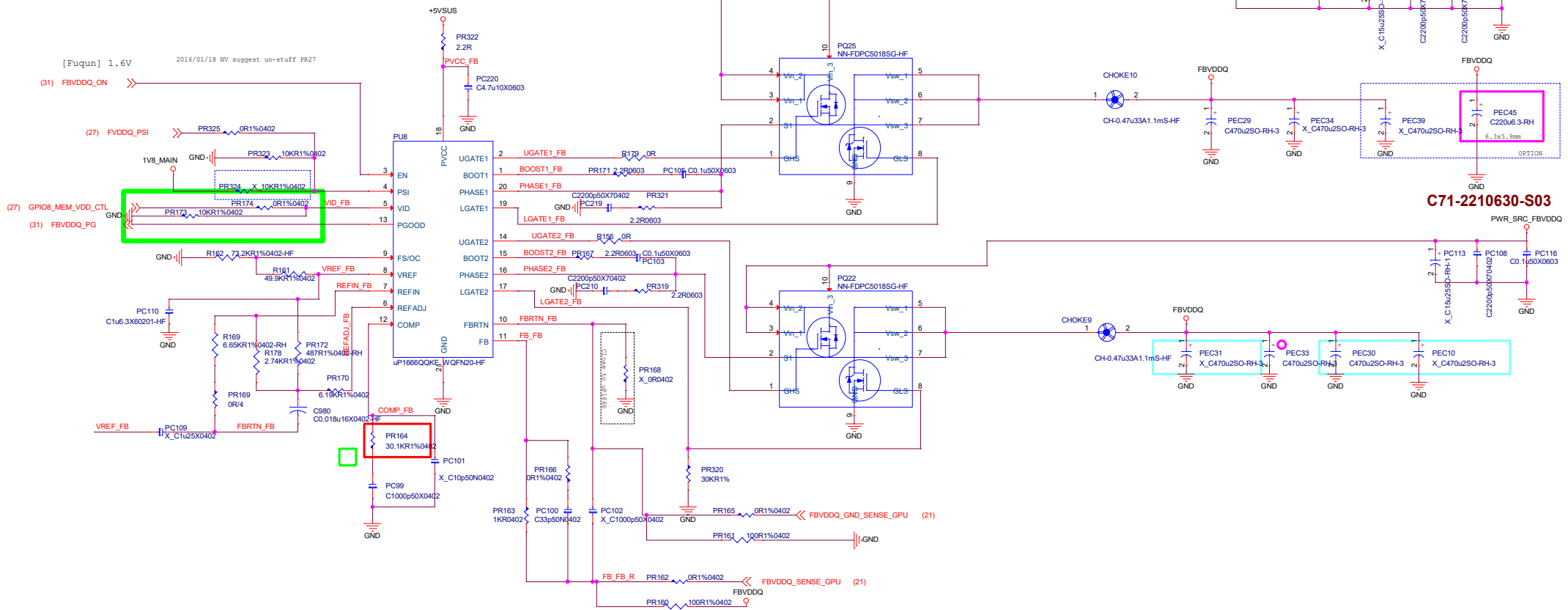
FBVDDQ POWER / UP1666P

EDP-Peak 74A

EDP-Con 28A

VBoot:1.35V

Vmin:1.25V / Vmax:1.35V



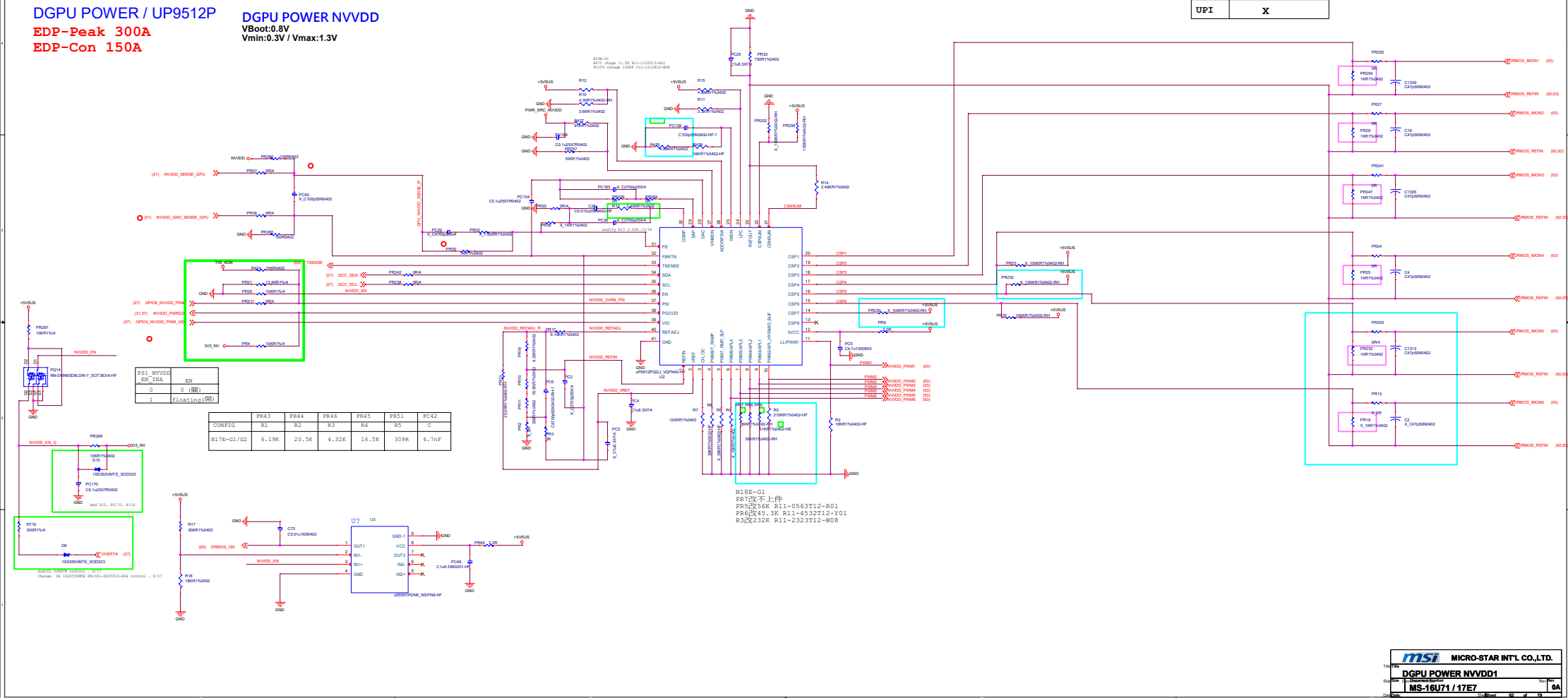
2016/01/18 NV suggest stuff PR278,PR279

msi MICRO-STAR INT'L CO.,LTD.			
Title DGPU POWER FBVDDQ1			
Size Document Number MS-16U71 / 17E7			
Date	Sheet	61 of 79	Rev 0A

EDP-Peak 300A
EDP-Con 150A

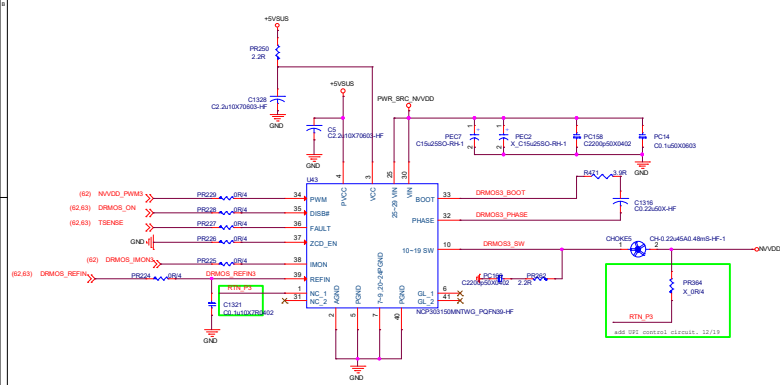
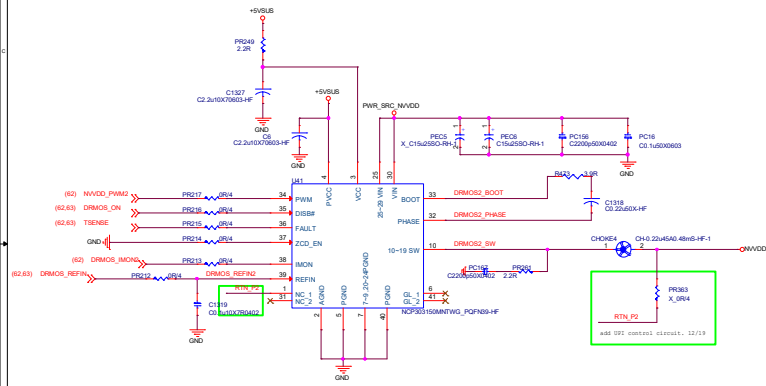
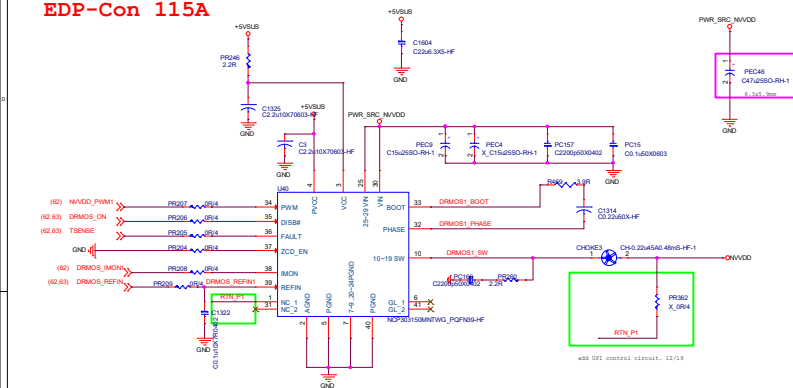
VBoot:0.8V
Vmin:0.3V / Vmax:1.3V

	99254, 99259, 99247, 9925, 99233, 9919
ON Semi	1K R11-0102T12-W08
UPI	X

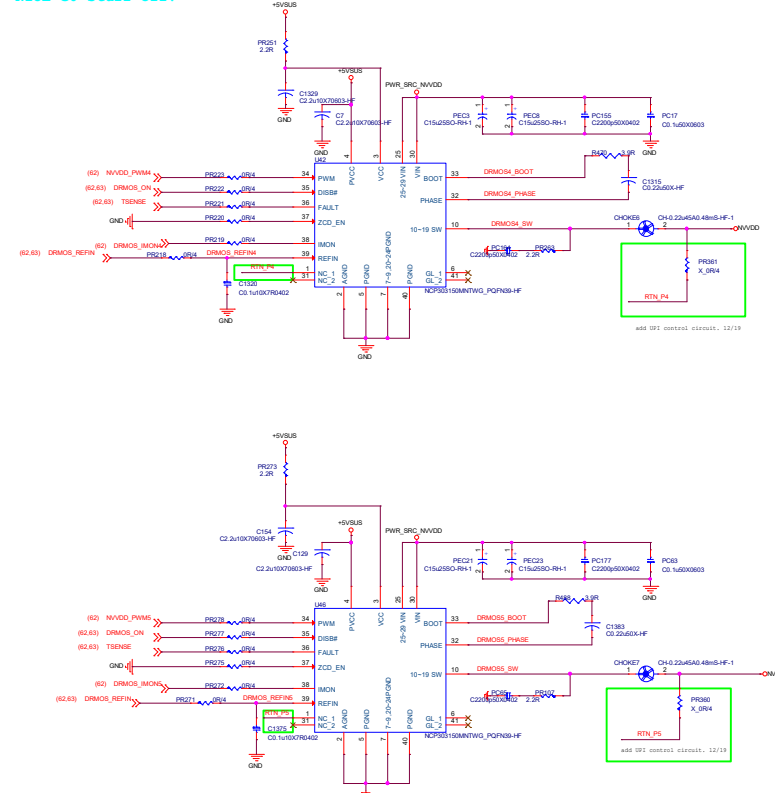


EDP-Peak 300A
EDP-Con 115A

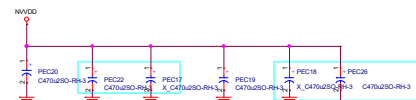
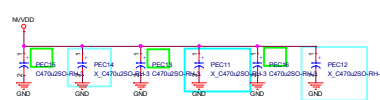
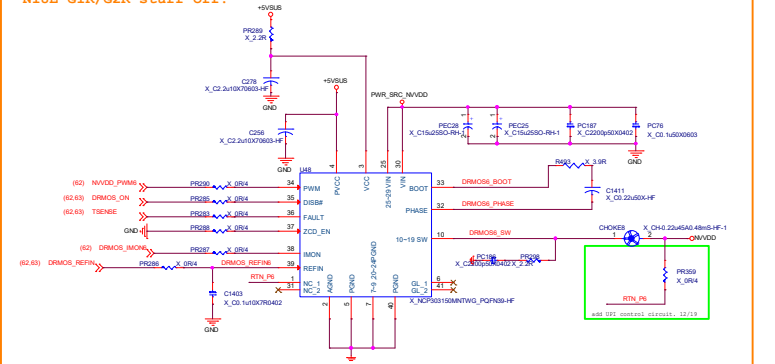
ON Semi	I33-303150C-005		8469, 8473, 8488, 8477, 8493, 8470	92359, 92365, 92361, 92362, 92363, 92364
UPI	I33-9619A0C-U47	ON Semi	3.9R R11-039A033-W08	X
		UPI	2.2R R11-022A013-W08	0R R11-0000012-W08

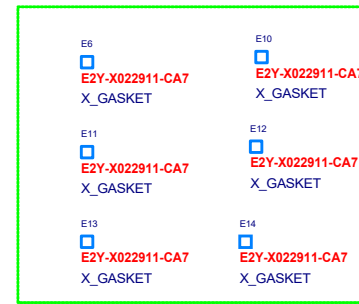
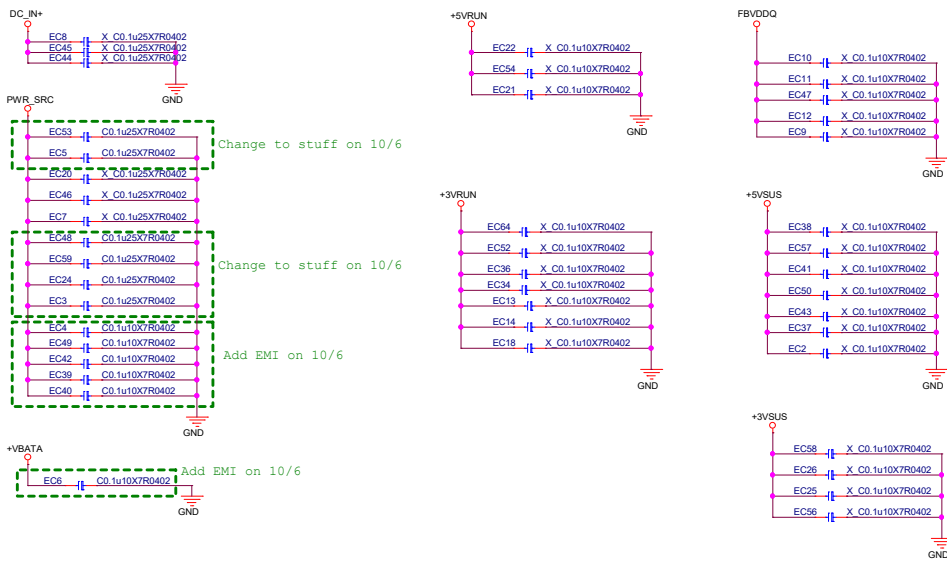


N18E-G0 stuff off.



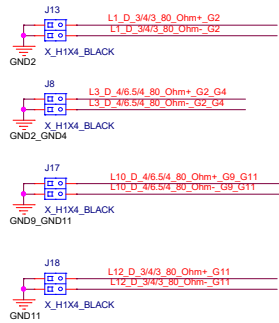
N18E-G1R/G2R stuff off.



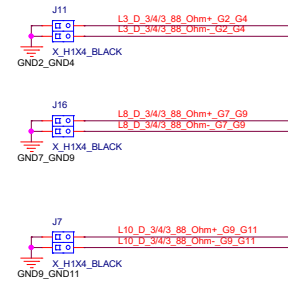


Add E4, E5, E6, E7, E8, E9 for EMI.5/22

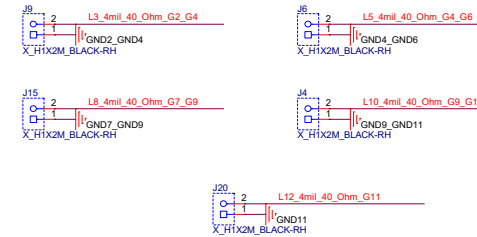
80 OHM / CLK/WCK/USB3.1



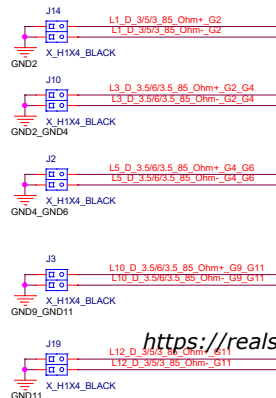
88 OHM /DDR4 CLK



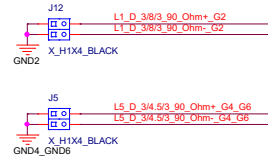
40 OHM / DDR4 CTRL



85 OHM /SATA /PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG

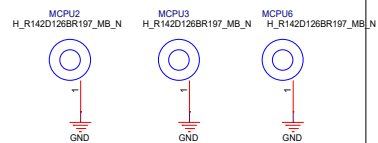


90 OHM LAN/USB 3.1 MUX

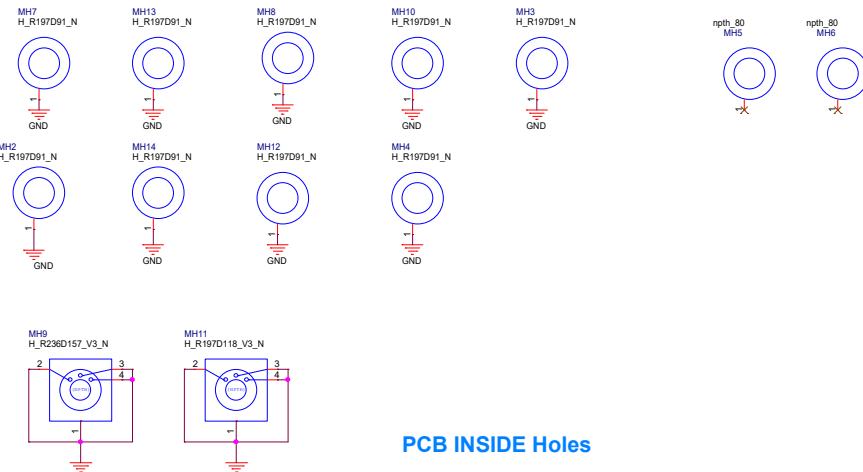
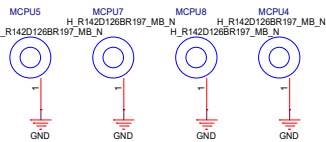


<https://realschematic.com>

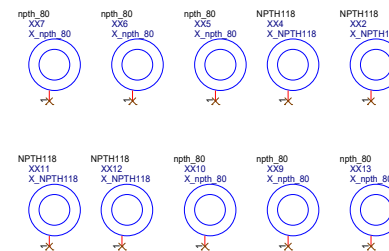
CPU Holes



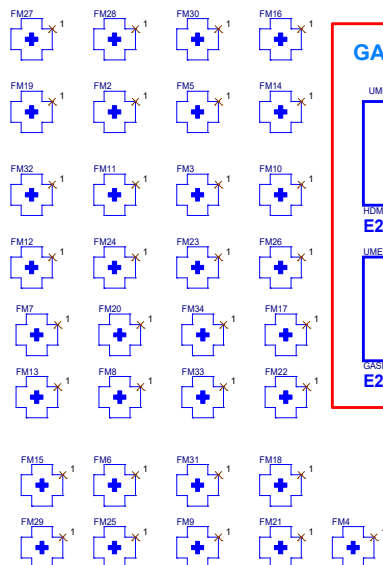
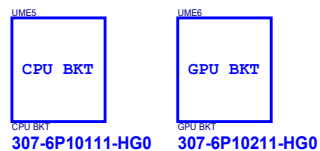
DGPU Holes



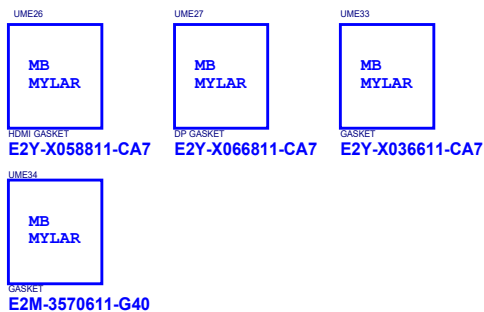
PCB INSIDE Holes



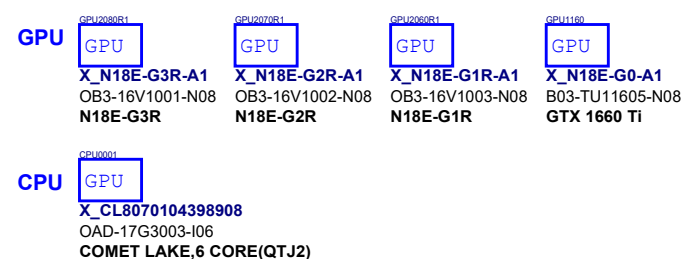
PCB OUTSIDE Holes



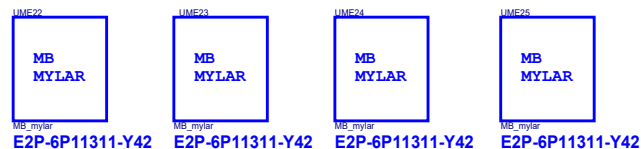
GASKET



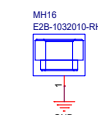
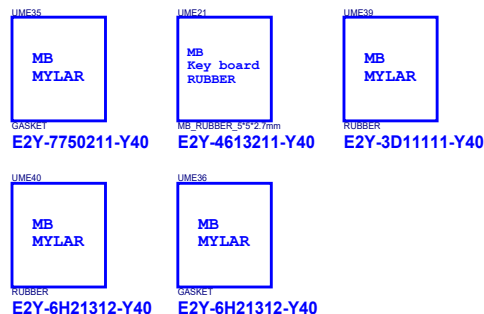
Option BOM 5020



MB_mylar



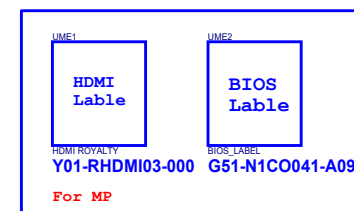
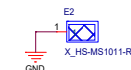
MB_RUBBER



1160	E2B-16P1020-A89
1170	E2B-1032010-A89
1180	E2B-16P1020-A89



PD0-16U710A-H73
TRIPOD: PD0-16U710A-T53



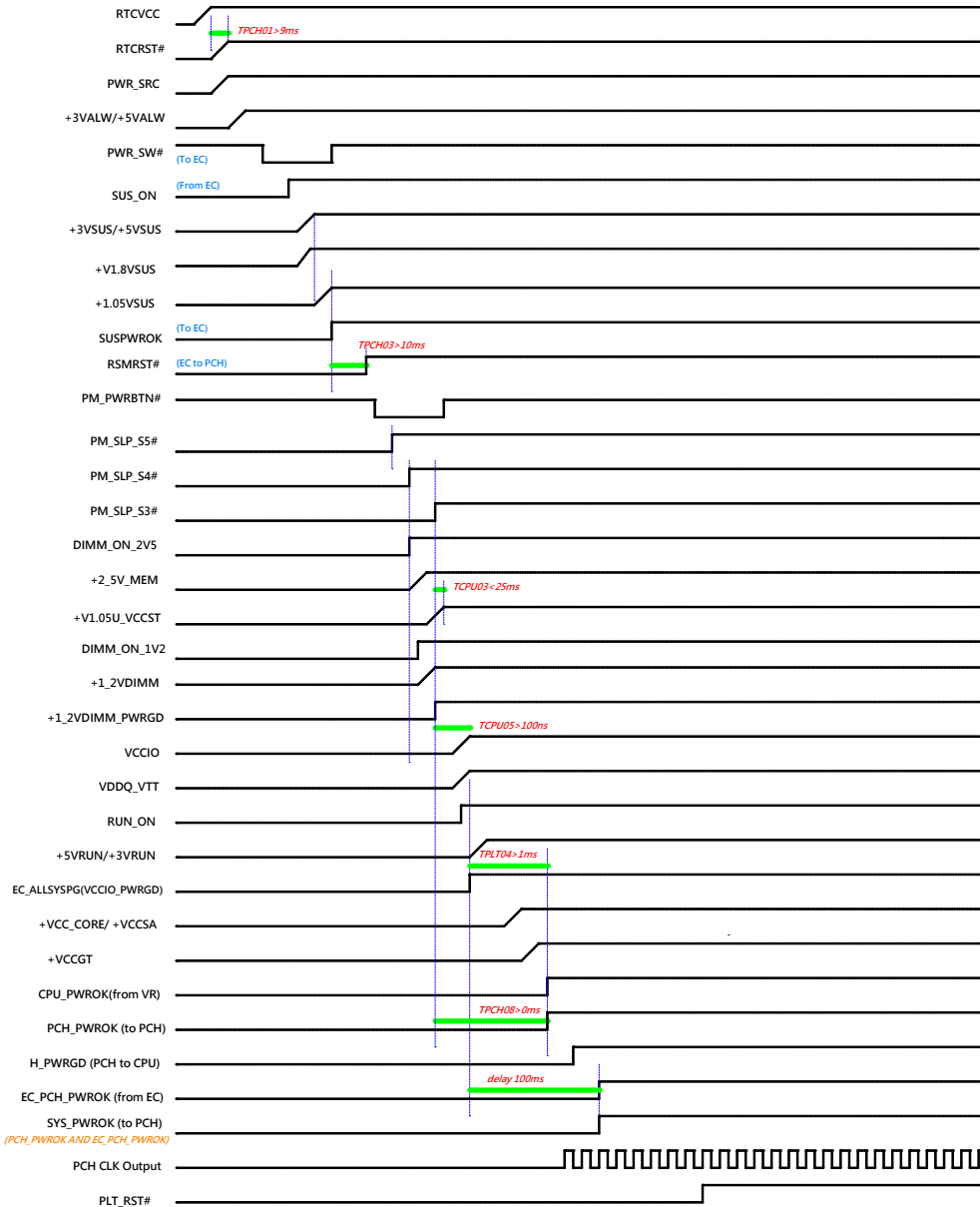
msi MICRO-STAR INT'L CO.,LTD.	
Screw/ME	
Document Number	MS-16U71 / 17E7
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<https://realschematic.com>

MS-16P1 Power Delivery Chart

Power on Sequence

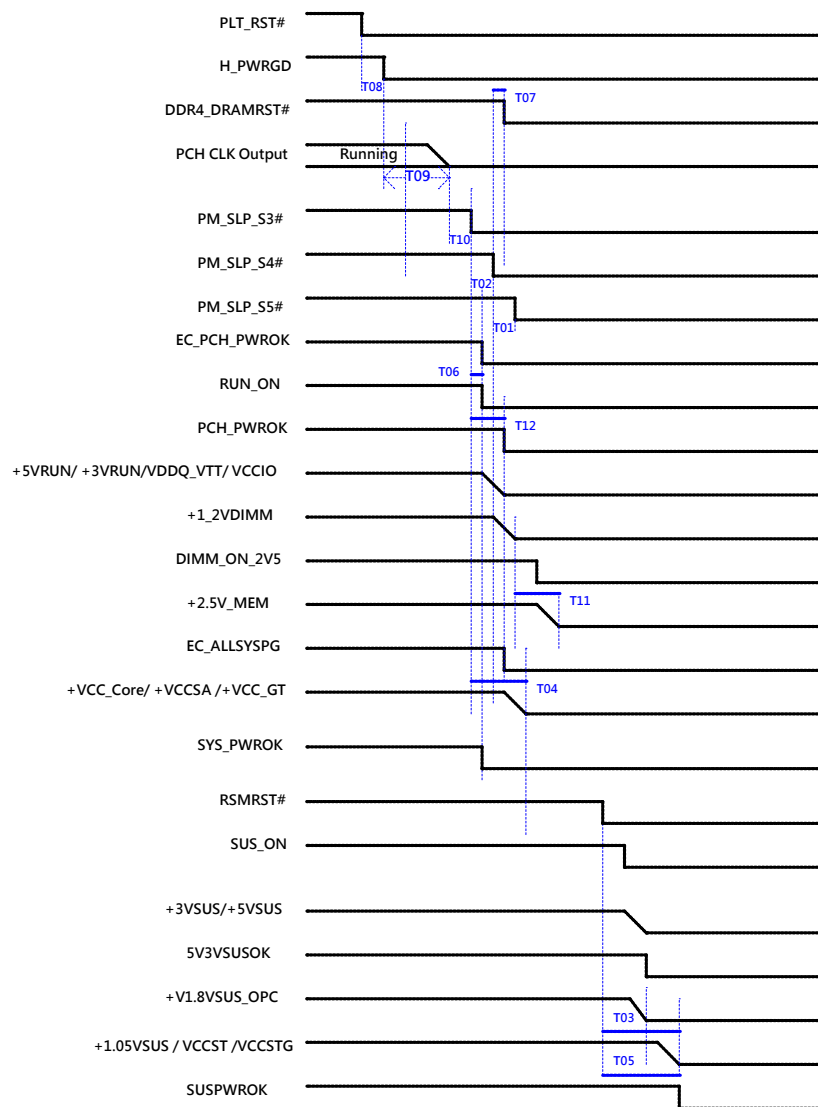
G3 -> S0



<https://realschematic.com>

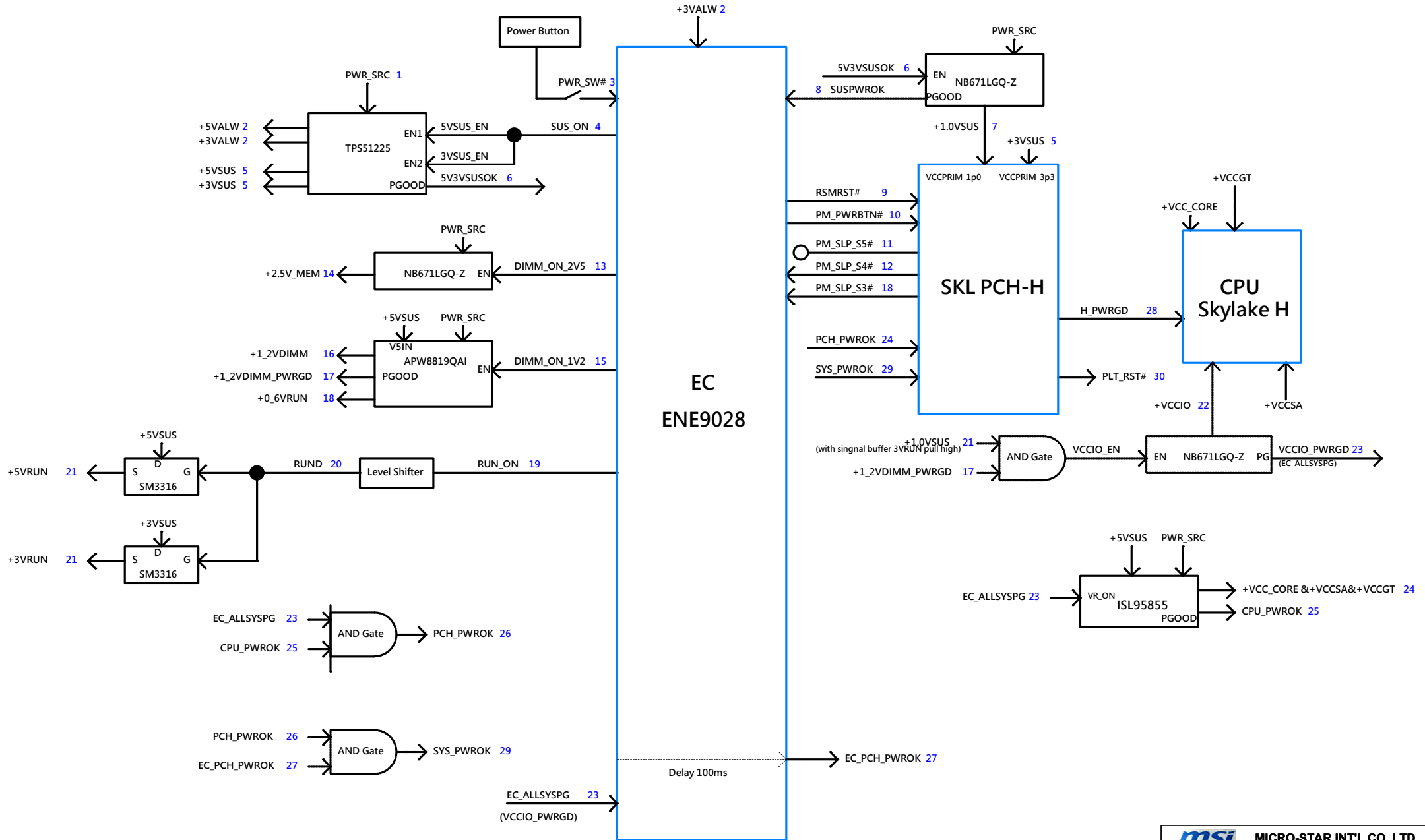
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-16P7 Power on Block Diagram



MS-16U7 Revision History List

2019/09/26 VER 0A MS-16U7_10_2070_SAMSUNG_i7-9750H_190925_1230_16_FINAL SENT TO LAYOUT.DSN
(Copy From MS-16U11)

Page XX (BOM) :Modify BOM FOLOW 607-16U11-05S (014)

2019/09/26 VER 0A MS-16U7_10_2070_SAMSUNG_i7-9750H_190926A.DSN

Page 5,6,7,58,59,60 (SCH) :Change CPU POWER Form 17E9

2019/09/26 VER 0A MS-16U7_10_2070_SAMSUNG_i7-9750H_190926B.DSN

Page 43 (LAYOUT) :Reduce HDMI2.0 Re-timer change to HDMI 1.4
Page 24 (BOM) :Reduce GPU Backside cap Form 47u*16 to 330u*2
Page 48 (LAYOUT) :Reduce USB 3.1 type A Re-timer
Page 42 (LAYOUT & BOM) :Add PEC52 For Costdown
Page 61 (LAYOUT & BOM) :Add PEC43 , PEC44 , PEC45 For Costdown
Page 63 (LAYOUT & BOM) :Add PEC46 For Costdown
Page 48,74 (LAYOUT) : Change EC55, ECB15, ECB11 form C11-4767314-M09 100uF 0805
to C71-101064G-S03 100uF TYPE B for USB ODD inrush current

2019/09/26 VER 0A MS-16U7_10_2070_SAMSUNG_i7-9750H_190926D.DSN

Page 50 (LAYOUT) : Delete Speaker
Page 51 (LAYOUT) : Delete WOOFER
Page 53 (LAYOUT) : Delete MOTO
Page 49 (LAYOUT) : CHANGE ALC1220 to ALC233

2019/10/03 VER 0A MS-16U7_10_2070_SAMSUNG_i7-9750H_191003A.DSN

Page 49 (LAYOUT) : Modify Audio Circuit for FAE request
Page 58 (BOM) : CHANGE PR4054 PR4265 PR4266 PR4267
Form R11-1743T22-Y01 to R11-1743T13-W08 for power request
Page 30 (BOM) : CHANGE U4
Form I37-454910C-O05 to I37-454920C-O05 for power request

2019/10/03 VER 0A MS-16U7_0A_2070_SAMSUNG_i7-9750H_19116C.DSN

Page 42 (BOM) : STUFF R160 and CHANGE PU9 PU11 U4036
Form I31-059300C-A30 to I31-059301C-A30 for design
Page 5 (BOM) : UnStuff C4089 , C4088 ,C4091 ,C4090 For Cost down